

MOSFET – Power, Single, N-Channel, SOT-23

30 V, 2.5 A

NTR4503N, NVTR4503N

Features

- Leading Planar Technology for Low Gate Charge / Fast Switching
- 4.5 V Rated for Low Voltage Gate Drive
- SOT-23 Surface Mount for Small Footprint (3 x 3 mm)
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC-DC Conversion
- Load/Power Switch for Portables
- Load/Power Switch for Computing

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DS}	30	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$	A
			$T_A = 85^\circ\text{C}$	
	$t \leq 10\text{ s}$	I_D	$T_A = 25^\circ\text{C}$	2.5
Power Dissipation (Note 1)	Steady State	P_D	$T_A = 25^\circ\text{C}$	W
			$T_A = 85^\circ\text{C}$	
Continuous Drain Current (Note 2)	Steady State	I_D	$T_A = 25^\circ\text{C}$	A
			$T_A = 85^\circ\text{C}$	
Power Dissipation (Note 2)		P_D	$T_A = 25^\circ\text{C}$	0.42
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$	I_{DM}	10	A
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	2.0	A
Peak Source Current (Diode Forward)	$t_p = 10\text{ }\mu\text{s}$	I_{SM}	4.0	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

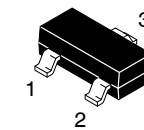
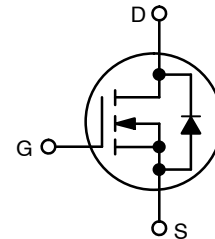
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	170	$^\circ\text{C/W}$
Junction-to-Ambient – $t < 10\text{ s}$ (Note 1)	$R_{\theta JA}$	100	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	300	

1. Surface-mounted on FR4 board using 1 in sq pad size.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

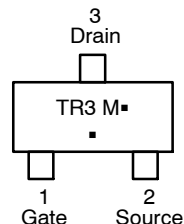
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	85 m Ω @ 10 V	2.5 A
	105 m Ω @ 4.5 V	

N-Channel



SOT-23
CASE 318
STYLE 21

MARKING DIAGRAM/ PIN ASSIGNMENT



TR3 = Specific Device Code
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTR4503NT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NVTR4503NT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

NTR4503N, NVTR4503N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	36		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1.0	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}, T_J = 125^\circ\text{C}$			10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0	1.75	3.0	V
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$		85	110	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 2.0\text{ A}$		105	140	
Forward Transconductance	g_{FS}	$V_{DS} = 4.5\text{ V}, I_D = 2.5\text{ A}$		5.3		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		135		pF
Output Capacitance	C_{oss}			52		
Reverse Transfer Capacitance	C_{rss}			15		
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 24\text{ V}$		130	250	pF
Output Capacitance	C_{oss}			42	75	
Reverse Transfer Capacitance	C_{rss}			13	25	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 2.5\text{ A}$		3.6	7.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate-to-Source Charge	Q_{GS}			0.6		
Gate-to-Drain Charge	Q_{GD}			0.7		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 24\text{ V}, I_D = 2.5\text{ A}$		1.9		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate-to-Source Charge	Q_{GS}			0.6		
Gate-to-Drain Charge	Q_{GD}			0.9		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V}, I_D = 1\text{ A}, R_G = 6\text{ }\Omega$		5.8	12	ns
Rise Time	t_r			5.8	10	
Turn-Off Delay Time	$t_{d(off)}$			14	25	
Fall Time	t_f			1.6	5.0	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 24\text{ V}, I_D = 2.5\text{ A}, R_G = 2.5\text{ }\Omega$		4.8		ns
Rise Time	t_r			6.7		
Turn-Off Delay Time	$t_{d(off)}$			13.6		
Fall Time	t_f			1.8		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 2.0\text{ A}$		0.85	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = 2.0\text{ A}, dI_S/dt = 100\text{ A}/\mu\text{s}$		9.2		ns
Reverse Recovery Charge	Q_{RR}			4.0		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.



TYPICAL PERFORMANCE CURVES

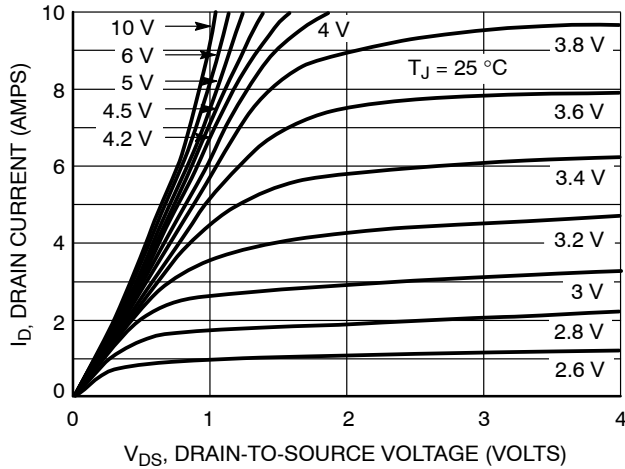


Figure 1. On-Region Characteristics

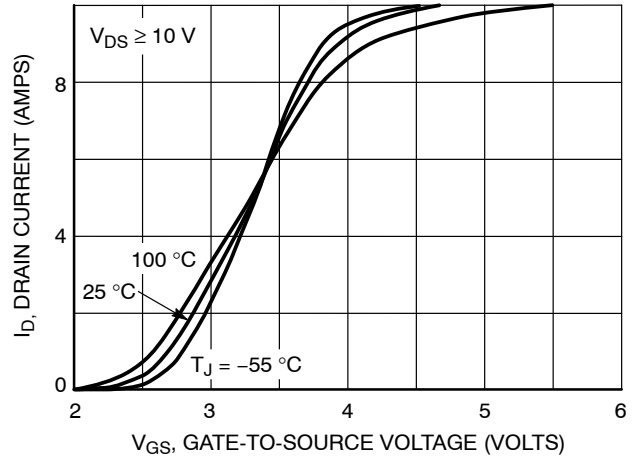


Figure 2. Transfer Characteristics

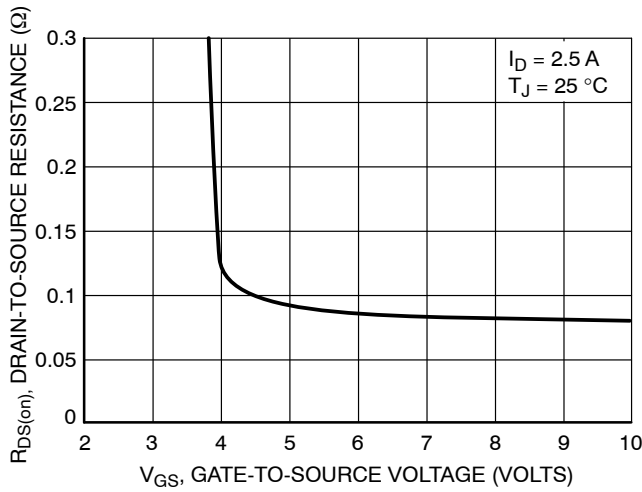


Figure 3. On-Resistance vs. Gate-to-Source Voltage

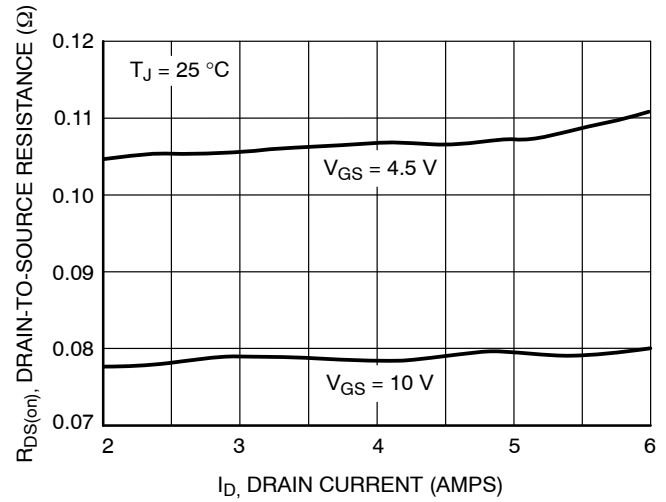


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

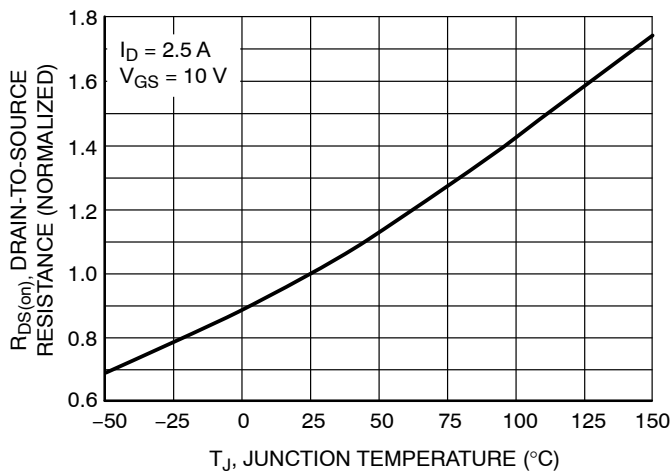


Figure 5. On-Resistance Variation with Temperature

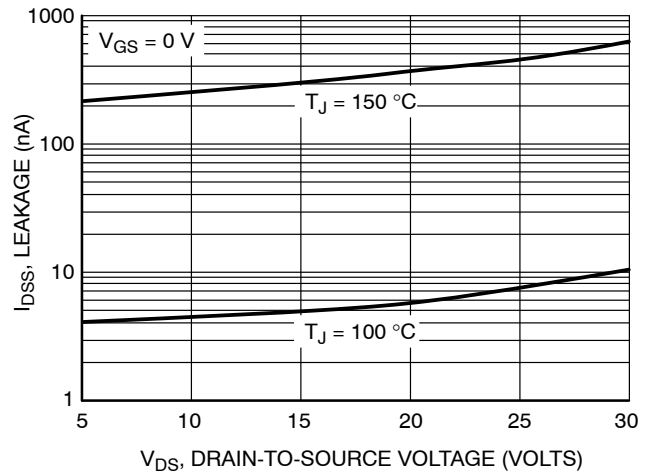


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

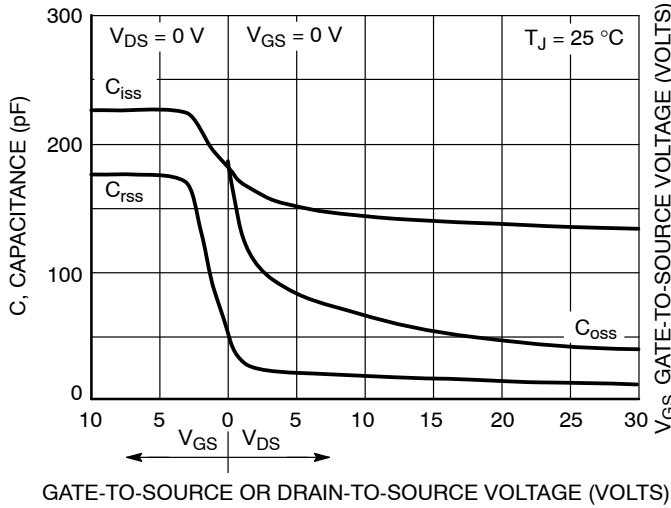


Figure 7. Capacitance Variation

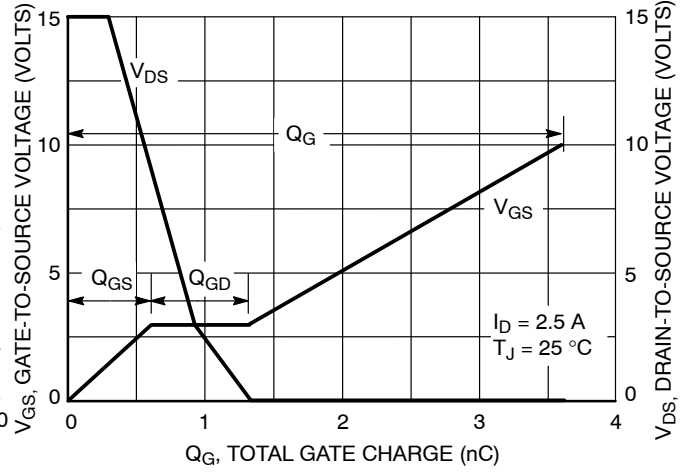


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

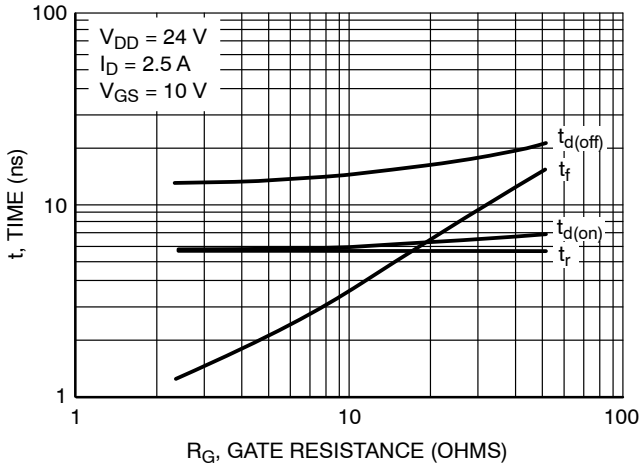


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

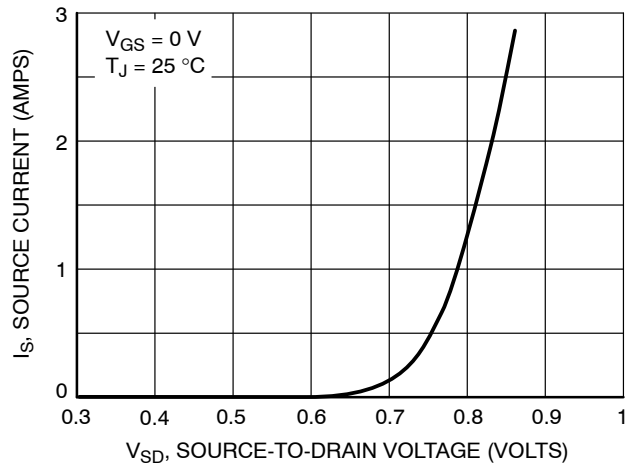


Figure 10. Diode Forward Voltage vs. Current

NTR4503N, NVTR4503N

REVISION HISTORY

Revision	Description of Changes	Date
9	Document rebranded to onsemi format.	2/17/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

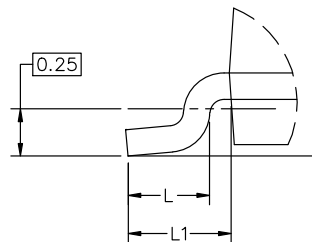
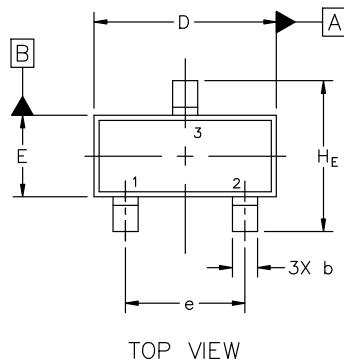




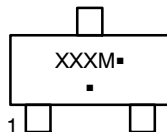
SCALE 4:1

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P
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ISSUE AU

DATE 14 AUG 2024

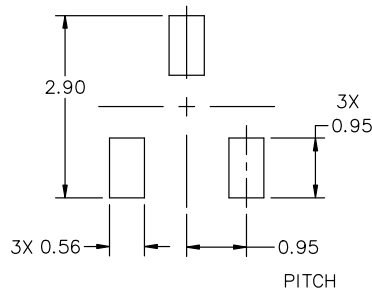


**GENERIC
MARKING DIAGRAM***



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

STYLES ON PAGE 2

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DATE 14 AUG 2024

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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