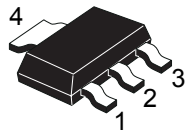
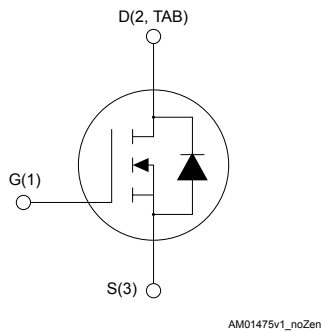


N-channel 100 V, 230 mΩ typ., 2.4 A STripFET II Power MOSFET in a SOT-223 package



SOT-223



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STN2NF10	100 V	260 mΩ	2.4 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching application
- DC-DC converters

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.



Product status link

[STN2NF10](#)

Product summary

Order code	STN2NF10
Marking	N2NF10
Package	SOT-223
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	2.4	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	1.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	17	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	3.3	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	30	V/ns
$E_{AS}^{(3)}$	Single-pulse avalanche energy	200	mJ
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 2.4\text{ A}$, $di/dt \leq 500\text{ A}/\mu\text{s}$, $V_{DD} = 80\text{ V}$.

3. $I_{AS} = 2.4\text{ A}$, $V_{DD} = 30\text{ V}$, $R_G = 4.7\text{ }\Omega$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	38	$^{\circ}\text{C}/\text{W}$

1. When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			10	
		$V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			1	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.2\text{ A}$		230	260	m Ω

1. Specified by design, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	280		pF
C_{oss}	Output capacitance		-	45		pF
C_{rss}	Reverse transfer capacitance		-	20		pF
Q_g	Total gate charge	$V_{DD} = 80\text{ V}$, $I_D = 2.4\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	10	14 ⁽¹⁾	nC
Q_{gs}	Gate-source charge		-	2.5		nC
Q_{gd}	Gate-drain charge		-	4		nC

1. Specified by design, not tested in production.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$, $I_D = 2.4\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	6	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	20	-	ns
t_f	Fall time		-	3	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		17	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.4 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 2.4 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 10 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	70		ns
Q_{rr}	Reverse recovery charge		-	175		nC
I_{RRM}	Reverse recovery current		-	5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

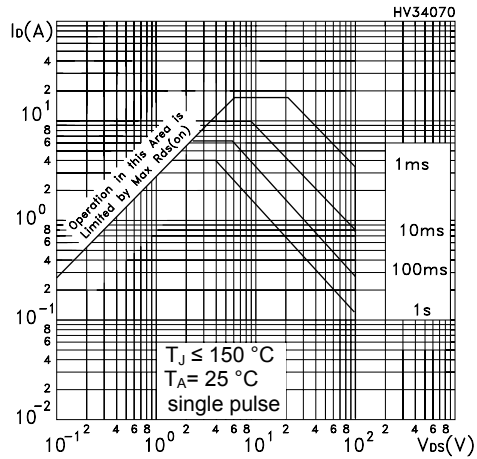


Figure 2. Thermal impedance

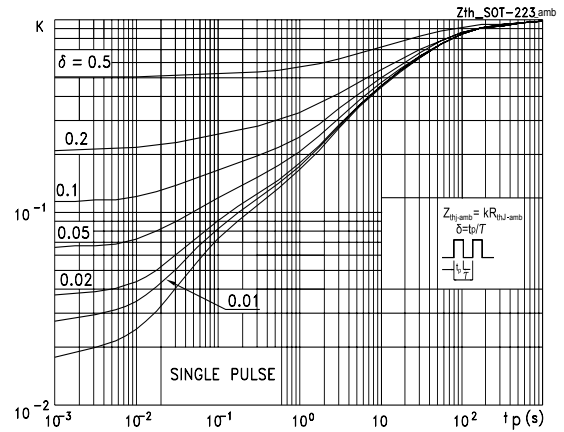


Figure 3. Output characteristics

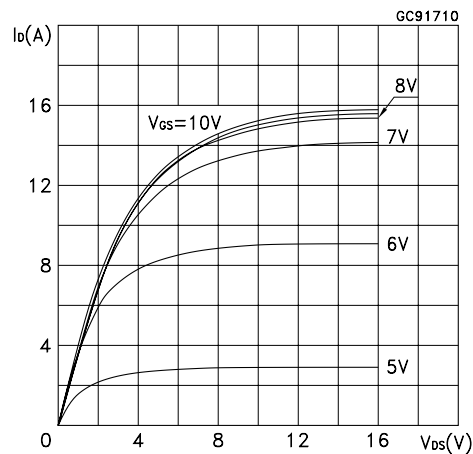


Figure 4. Transfer characteristics

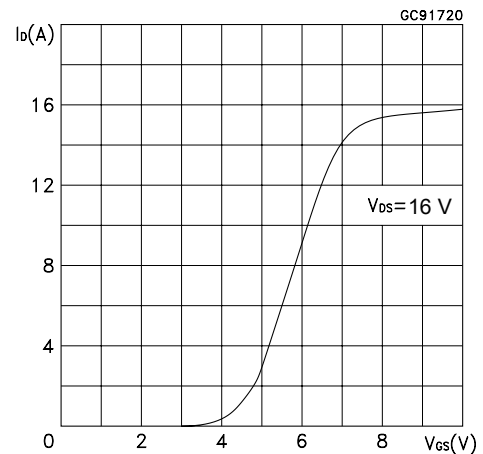


Figure 5. Static drain-source on-resistance

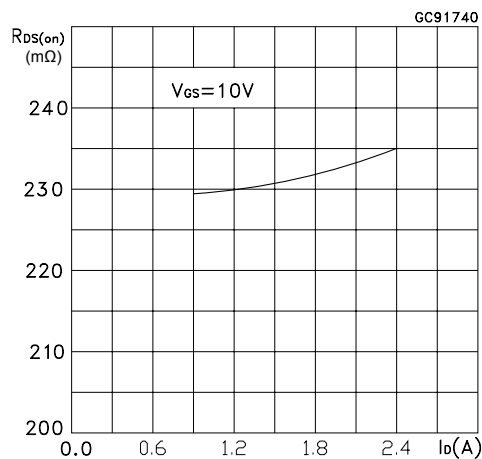


Figure 6. Gate charge vs gate-source voltage

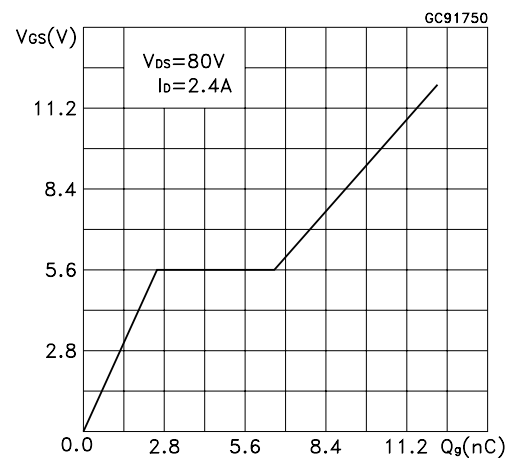


Figure 7. Capacitance variations

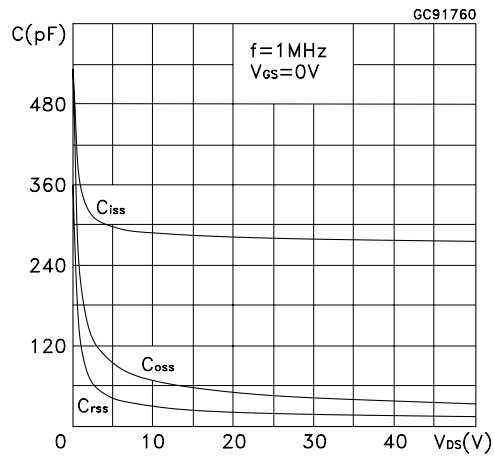


Figure 8. Normalized gate threshold voltage vs temperature

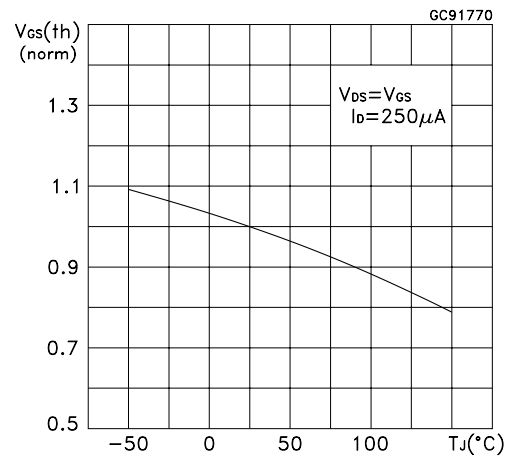


Figure 9. Normalized on-resistance vs temperature

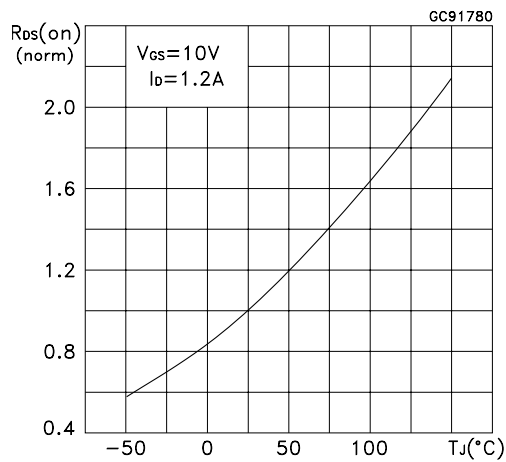


Figure 10. Typical reverse diode forward characteristics

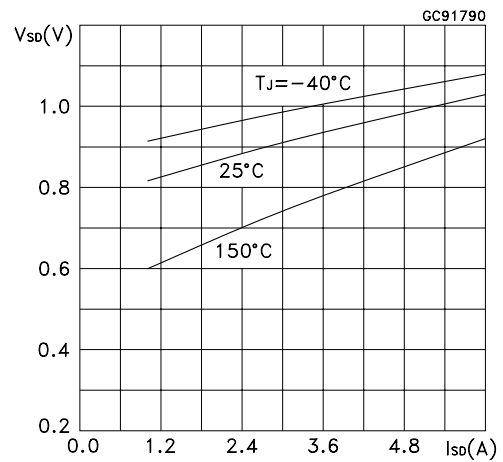
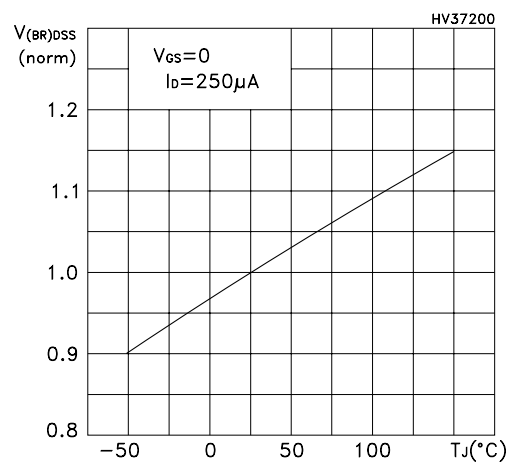


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 12. Test circuit for resistive load switching times


AM01468v1

Figure 13. Test circuit for gate charge behavior


AM01469v1

Figure 14. Test circuit for inductive load switching and diode recovery times


AM01470v1

Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform

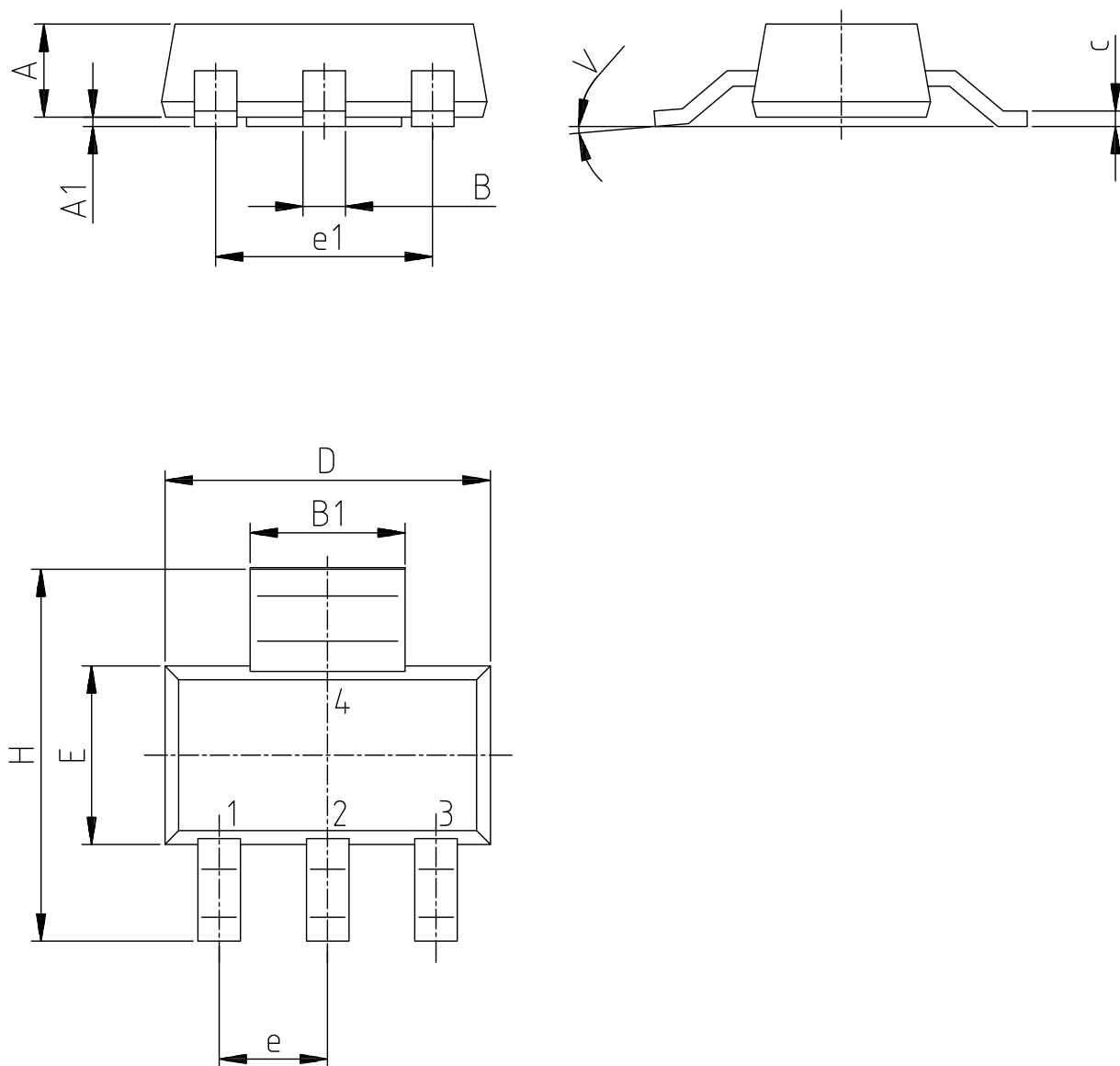

AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SOT-223 package information

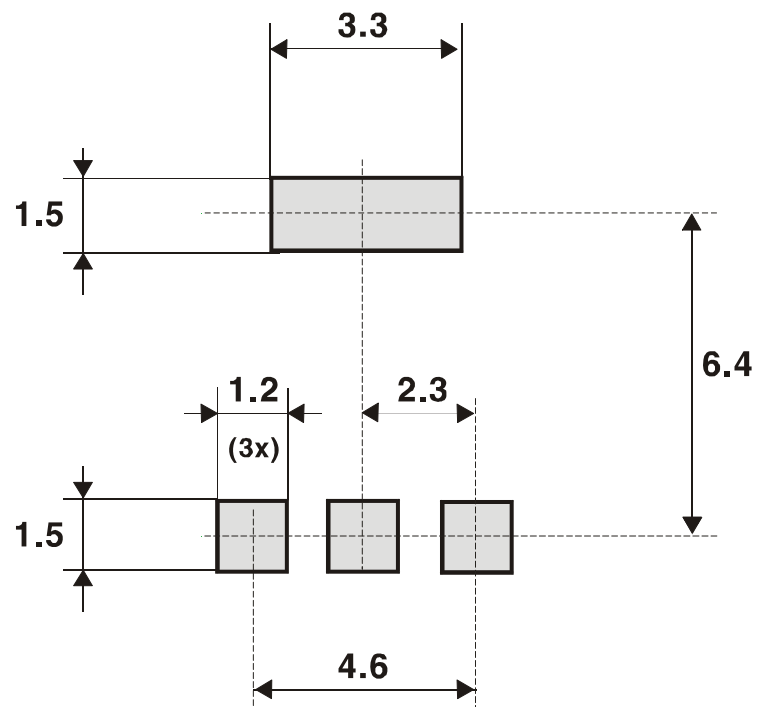
Figure 18. SOT-223 package outline



0046067_15

Table 7. SOT-223 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.8
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7	7.3
V			10 deg
A1	0.02		0.1

Figure 19. SOT-223 recommended footprint (dimensions are in mm)


0046067

4.2 SOT-223 packing information

Figure 20. SOT-223 tape outline

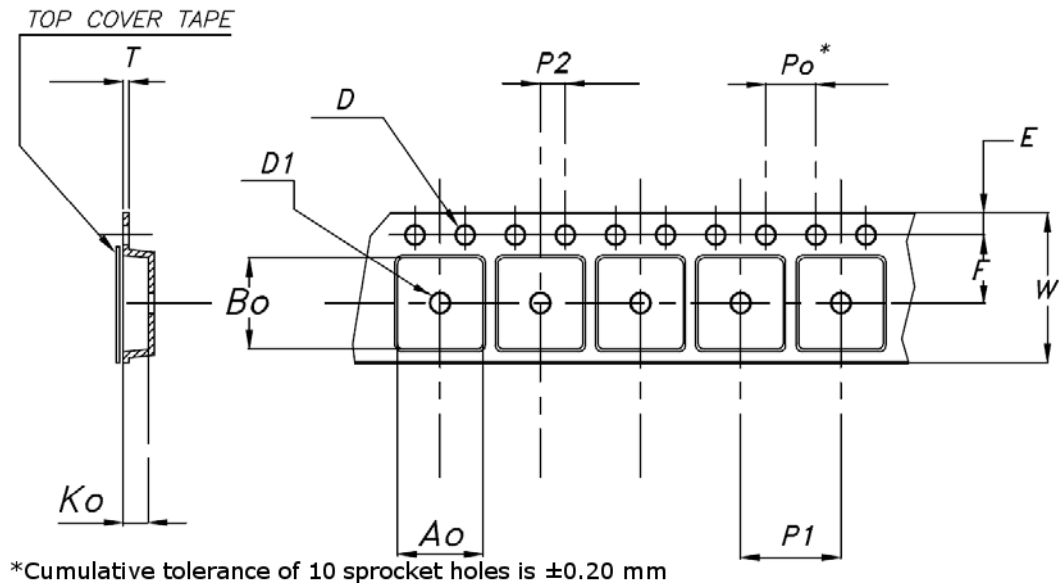


Figure 21. SOT-223 reel outline

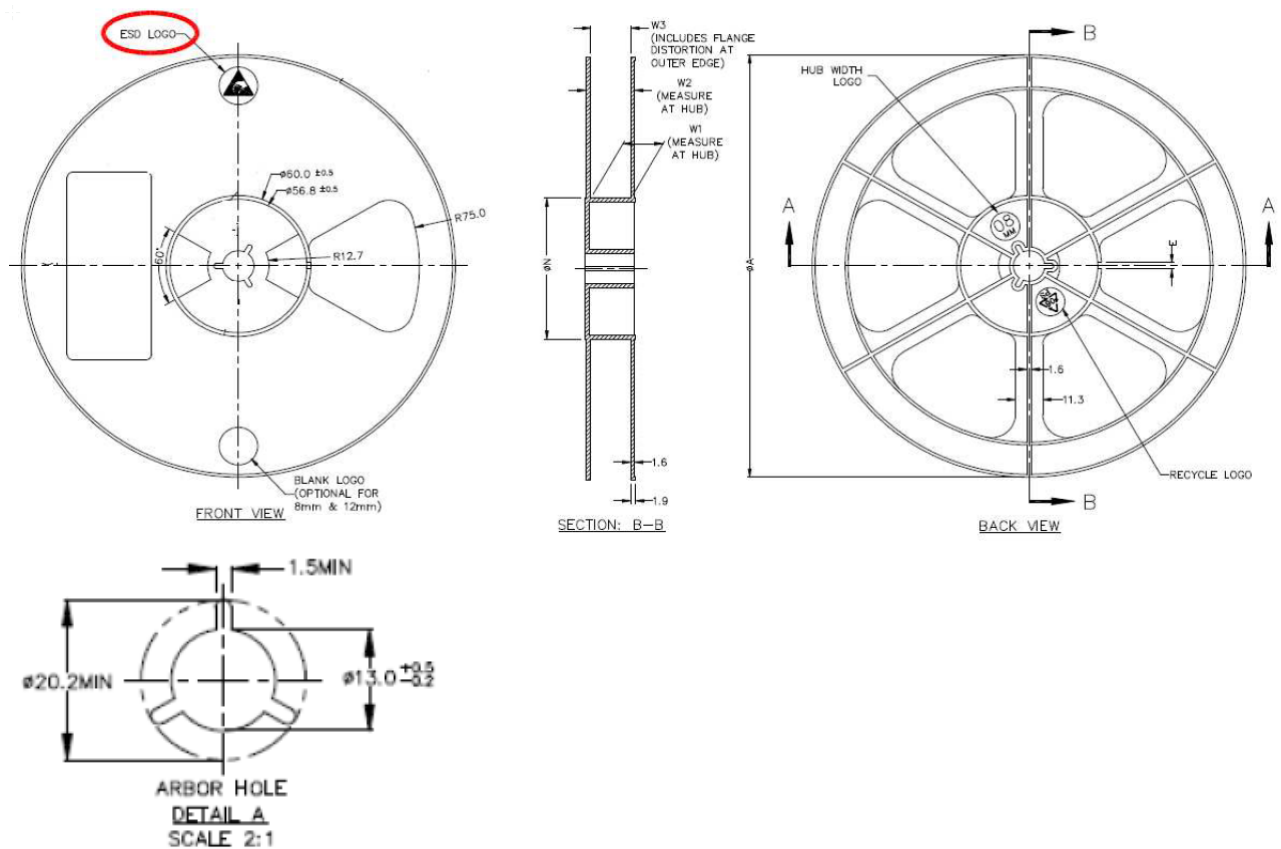


Table 8. SOT-223 tape and reel mechanical data

Tape				Tape		
Dim.	mm			Dim.	mm	
	Min.	Typ.	Max.		Min.	Max.
A0	6.75	6.85	6.95	A		180
B0	7.30	7.40	7.50	N	60	
K0	1.80	1.90	2.00	W1		12.4
F	5.40	5.50	5.60	W2		18.4
E	1.65	1.75	1.85	W3	11.9	15.4
W	11.7	12.0	12.3			
P2	1.90	2.00	2.10	Base quantity pcs		1000
P0	3.90	4.00	4.10	Bulk quantity pcs		1000
P1	7.90	8.00	8.10			
T	0.25	0.30	0.35			
DΦ	1.50	1.55	1.60			
D1Φ	1.50	1.60	1.70			

Revision history

Table 9. Document revision history

Date	Version	Changes
14-Sep-2006	4	The document has been reformatted
29-Mar-2007	5	<i>Figure 1</i> has been updated
04-Apr-2007	6	New test condition for I_{DSS} on <i>Table 3</i>
10-Jun-2026	7	Updated Section 2.1: Electrical characteristics (curves) and Section 4: Package information . Minor text changes.

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