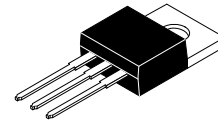


MOSFET – N-Channel, POWERTRENCH®

105 V, 41 A, 33 mΩ

FDP3672



TO-220-3LD
CASE 340AT

Features

- $R_{DS(on)} = 25 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 41 \text{ A}$
- $Q_{G(tot)} = 28 \text{ nC}$ (Typ.) @ $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low Q_{rr} Body Diode
- Optimized Efficiency at High Frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)

Applications

- Consumer Appliances
- Synchronous Rectification
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

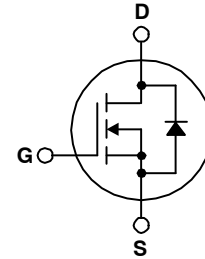
MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	105	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$) Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 10 \text{ V}$) Continuous ($T_{amb} = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$, $R_{\theta JA} = 62^\circ\text{C/W}$) Pulsed	41 31 5.9 Fig. 4	A
E_{AS}	Single Pulsed Avalanche Energy (Note 1)	48	mJ
P_D	Power Dissipation Derate above 25°C	135 0.9	W W/ $^\circ\text{C}$
T_J , T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

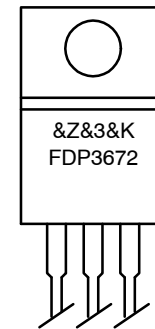
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.11	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 2)	62	



MARKING DIAGRAM



&Z = Assembly Location
&3 = Date Code (Year & Week)
&K = Lot Run Traceability Code
FDP3672 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FDP3672	TO-220-3LD	800 Units / Tube

FDP3672

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	105	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}$	–	–	1	μA
		$V_{GS} = 0\ \text{V}$, $T_C = 150^\circ\text{C}$	–	–	250	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2	–	4	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 41\ \text{A}$, $V_{GS} = 10\ \text{V}$	–	0.025	0.033	Ω
		$I_D = 21\ \text{A}$, $V_{GS} = 6\ \text{V}$	–	0.031	0.055	
		$I_D = 41\ \text{A}$, $V_{GS} = 10\ \text{V}$, $T_C = 175^\circ\text{C}$	–	0.063	0.070	

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	1670	–	pF
C_{oss}	Output Capacitance		–	240	–	
C_{rss}	Reverse Transfer Capacitance		–	55	–	
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_D = 41\ \text{A}$, $I_G = 1.0\ \text{mA}$	–	28	37	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0\ \text{V}$ to $2\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_D = 41\ \text{A}$, $I_G = 1.0\ \text{mA}$	–	3.9	5	
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 50\ \text{V}$, $I_D = 41\ \text{A}$, $I_G = 1.0\ \text{mA}$	–	12	–	
Q_{gs2}	Gate Charge Threshold to Plateau		–	8.0	–	
Q_{gd}	Gate to Drain "Miller" Charge		–	6.5	–	

RESISTIVE SWITCHING CHARACTERISTICS ($V_{GS} = 10\ \text{V}$)

$t_{(on)}$	Turn-On Time	$V_{DD} = 50\ \text{V}$, $I_D = 41\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GS} = 11.0\ \Omega$	–	–	90	ns
$t_{d(on)}$	Turn-On Delay Time		–	12	–	
t_r	Rise Time		–	48	–	
$t_{d(off)}$	Turn-Off Delay Time		–	24	–	
t_f	Fall Time		–	27	–	
$t_{(off)}$	Turn-Off Time		–	–	77	

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 41\ \text{A}$	–	–	1.25	V
		$I_{SD} = 21\ \text{A}$	–	–	1.0	
t_{rr}	Reverse Recovery Time	$I_{SD} = 41\ \text{A}$, $dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$	–	–	39	ns
Q_{rr}	Reverse Recovered Charge	$I_{SD} = 41\ \text{A}$, $dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$	–	–	42	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- Starting $T_J = 25^\circ\text{C}$, $L = 0.11\ \text{mH}$, $I_{AS} = 30\ \text{A}$.
- Pulse Width = 100 s.



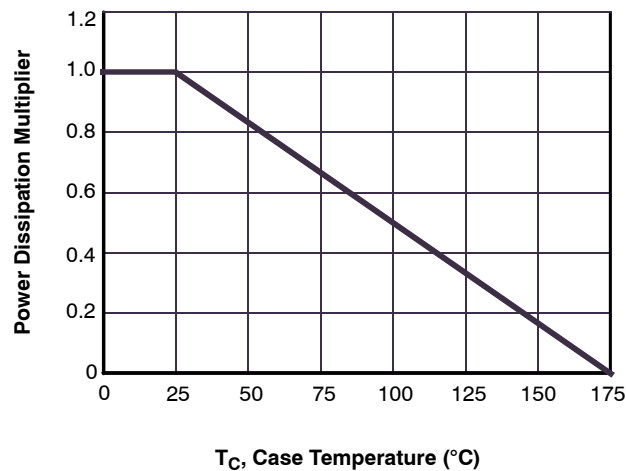
TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Figure 2. Normalized Power Dissipation vs Ambient Temperature

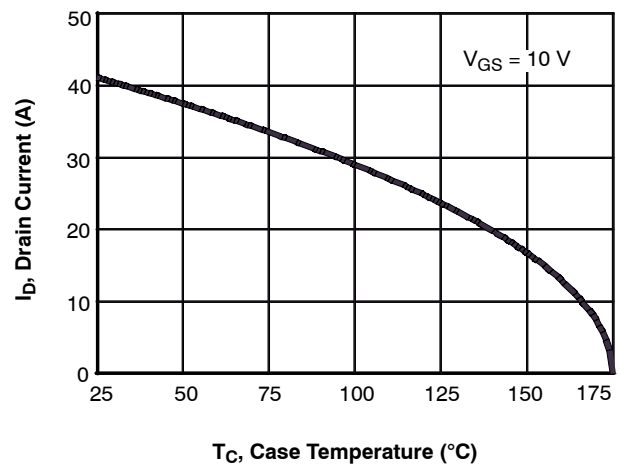


Figure 1. Maximum Continuous Drain Current vs Case Temperature

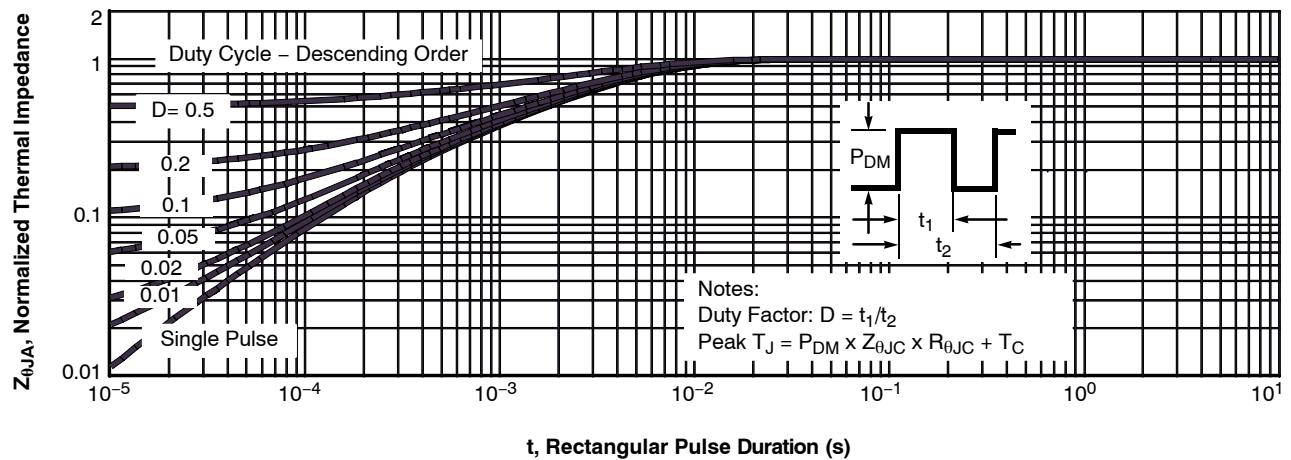


Figure 3. Normalized Maximum Transient Thermal Impedance

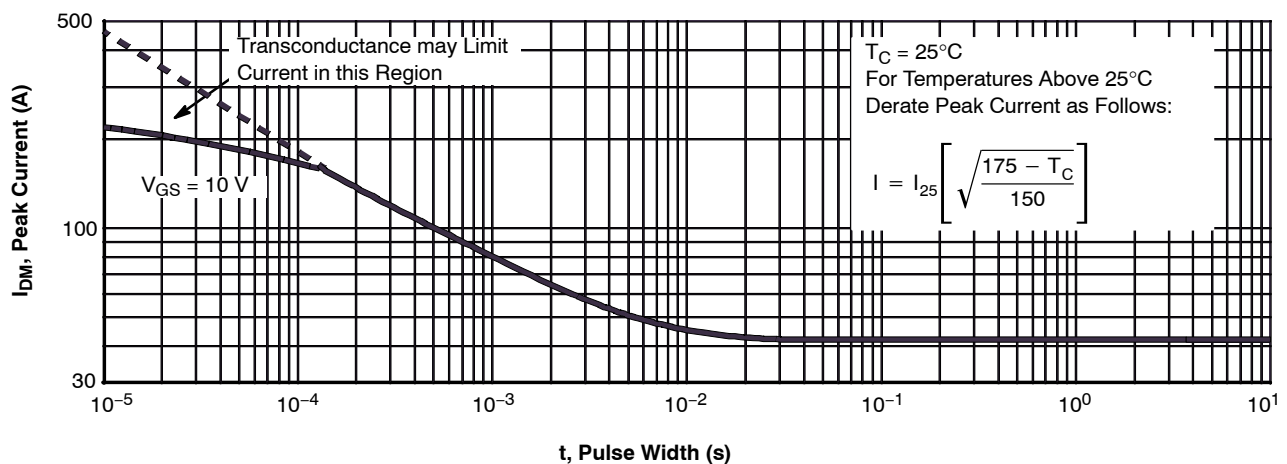


Figure 4. Peak Current Capability

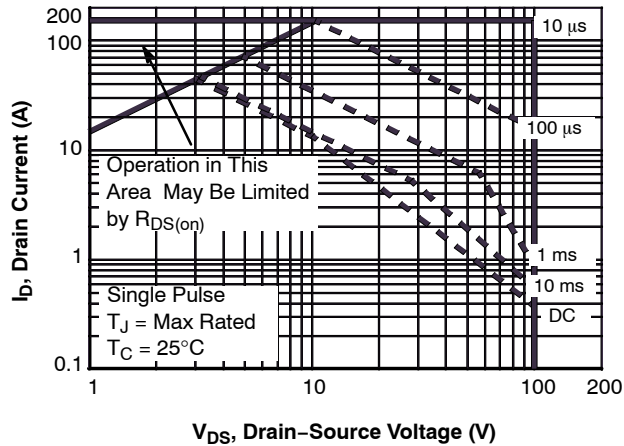
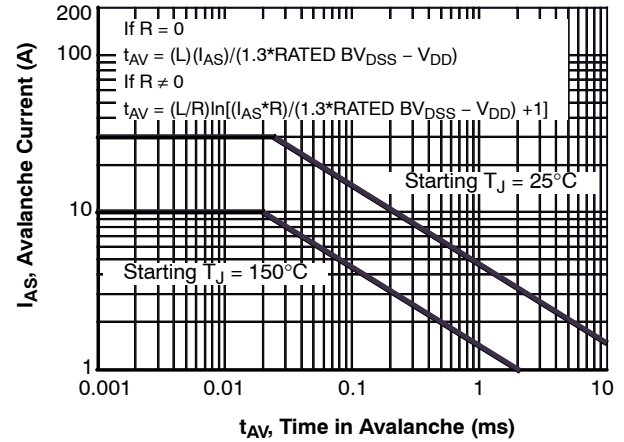
TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Figure 5. Forward Bias Safe Operating Area



NOTES: Refer to Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

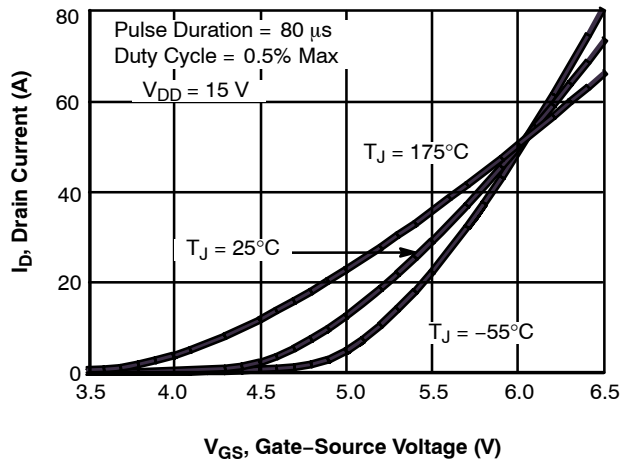


Figure 7. Transfer Characteristics

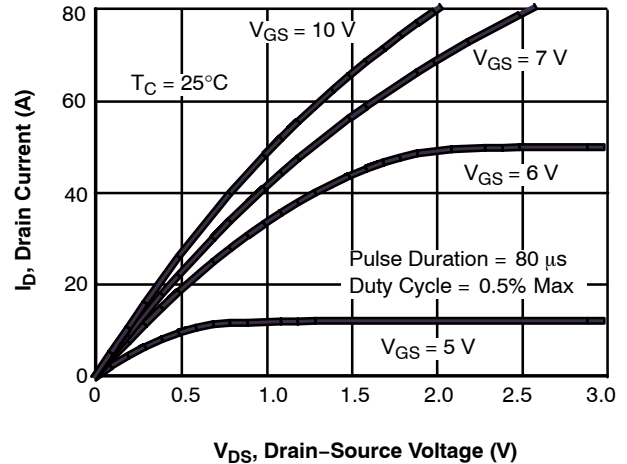


Figure 8. Saturation Characteristics

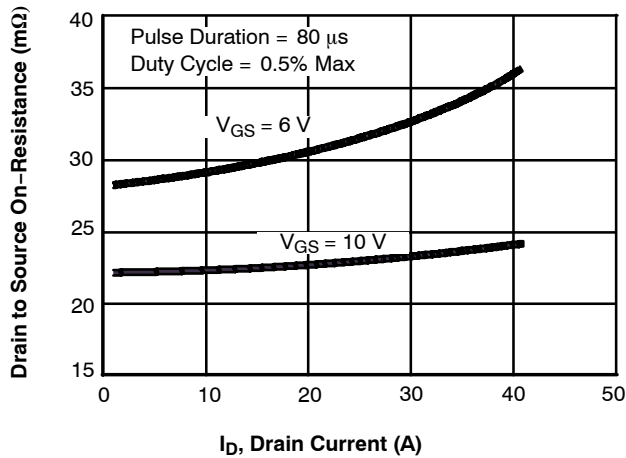


Figure 9. Drain to Source On Resistance vs. Drain Current

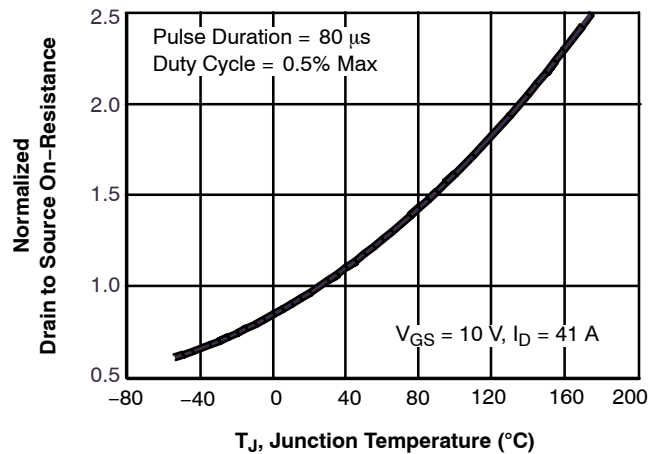


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

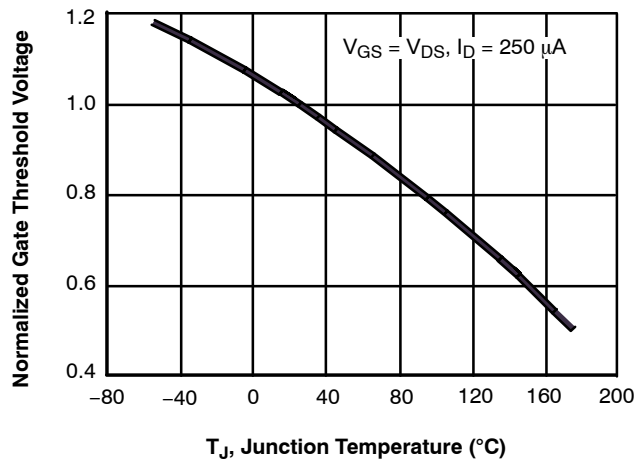
TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

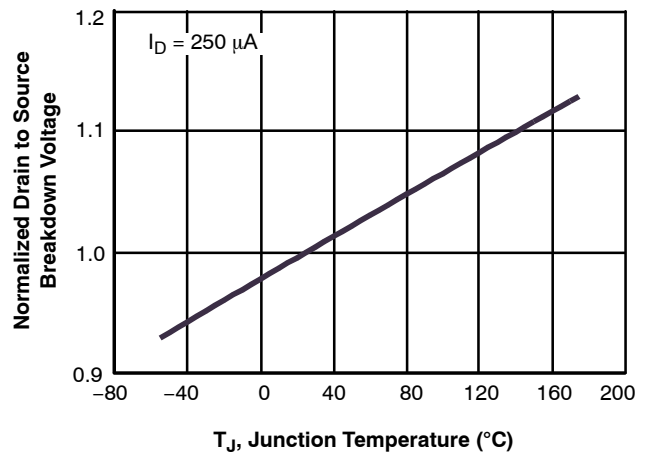


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

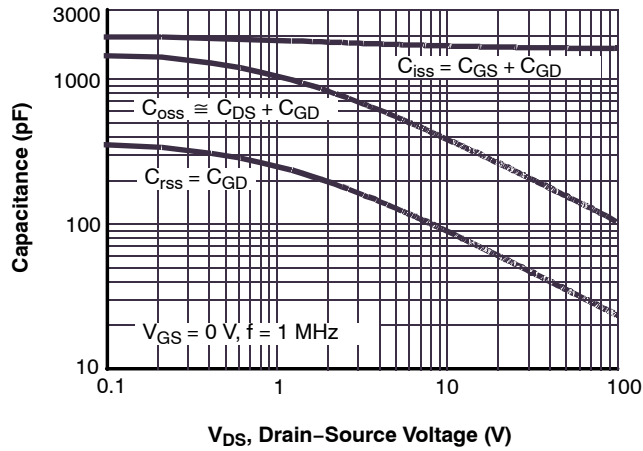


Figure 13. Capacitance vs Drain to Source Voltage

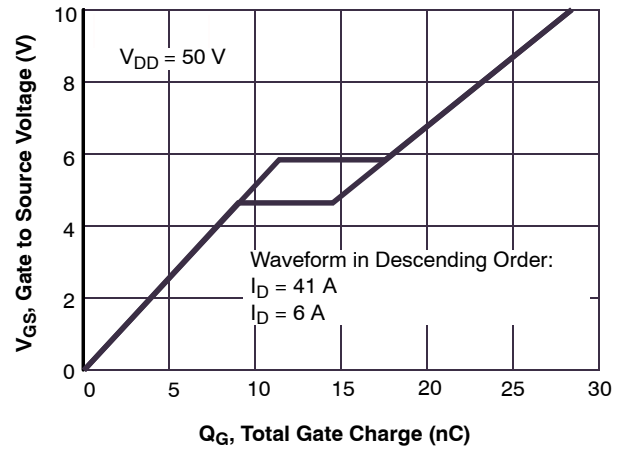


Figure 14. Gate Charge Waveforms for Constant Gate Currents

TEST CIRCUITS AND WAVEFORMS

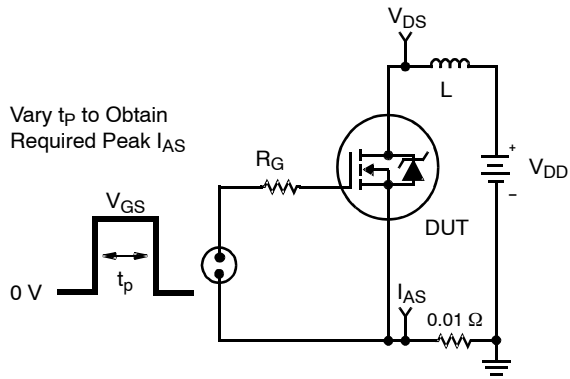


Figure 15. Unclamped Energy Test Circuit

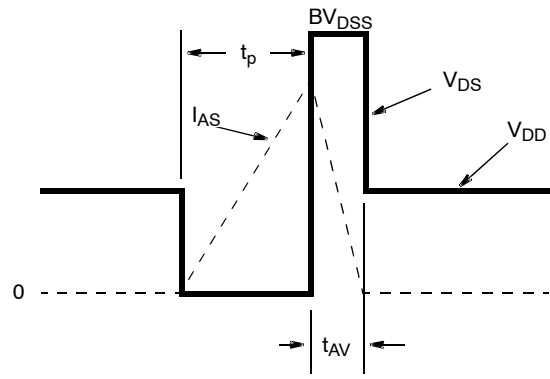


Figure 16. Unclamped Energy Waveforms

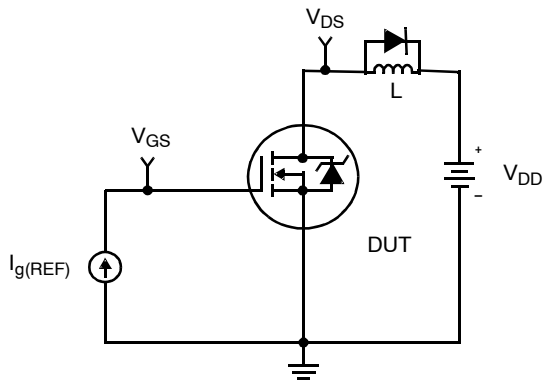


Figure 17. Gate Charge Test Circuit

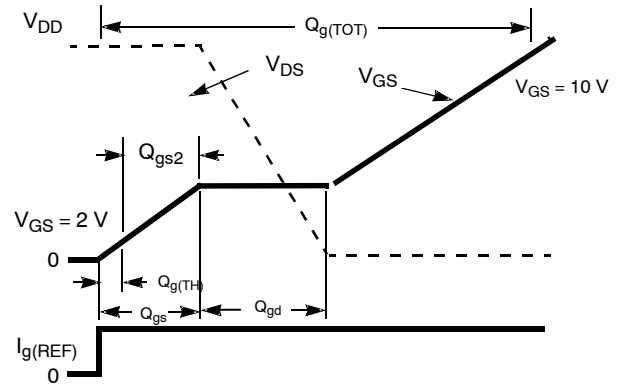


Figure 18. Gate Charge Waveforms

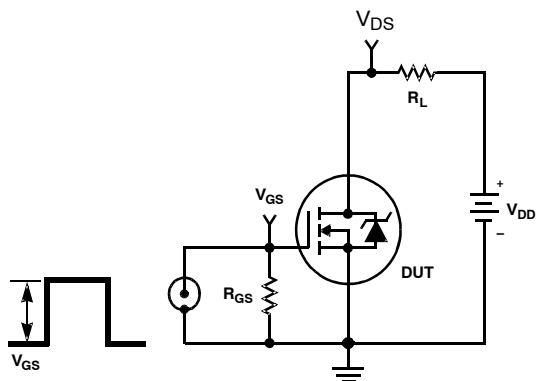


Figure 19. Switching Time Test Circuit

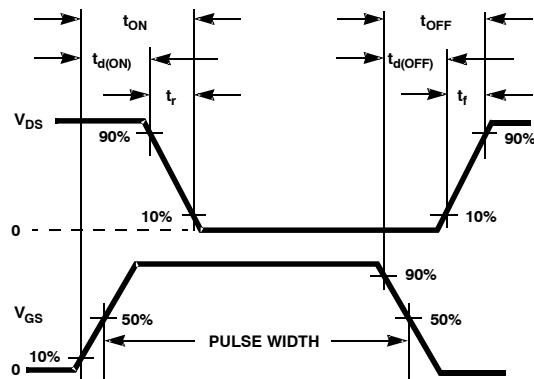


Figure 20. Switching Time Waveforms

FDP3672

PSPICE ELECTRICAL MODEL

.SUBCKT FDP3672 2 1 3 ; rev October 2002

Ca 12 8 5.8e-10

Cb 15 14 6.8e-10

Cin 6 8 1.6e-9

Dbody 7 5 DbodyMOD

Dbreak 5 11 DbreakMOD

Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 105

Eds 14 8 5 8 1

Egs 13 8 6 8 1

Esg 6 10 6 8 1

Evthres 6 21 19 8 1

Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 9.56e-9

Ldrain 2 5 1.0e-9

Lsource 3 7 4.45e-9

RLgate 1 9 95.6

RLdrain 2 5 10

RLsource 3 7 44.5

Mmed 16 6 8 8 MmedMOD

Mstro 16 6 8 8 MstroMOD

MweakMOD 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1

Rdrain 50 16 RdrainMOD 6.0e-3

Rgate 9 20 1.5

RSLC1 5 51 RSLCMOD 1.0e-6

RSLC2 5 50 1.0e3

Rsource 8 7 RsourceMOD 9.5e-3

Rvthres 22 8 RvthresMOD 1

Rvtemp 18 19 RvtempMOD 1

S1a 6 12 13 8 S1AMOD

S1b 13 12 13 8 S1BMOD

S2a 6 15 14 13 S2AMOD

S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) * (PWR(V(5,51)/(1e-6*98),3)) }

.MODEL DbodyMOD D (IS=1.0E-11 N=1.05 RS=3.7e-3 TRS1=2.5e-3 TRS2=1.0e-6
+ CJO=1.2e-9 M=0.58 TT=3.75e-8 XTI=4.0)

.MODEL DbreakMOD D (RS=15 TRS1=4.0e-3 TRS2=-5.0e-6)

.MODEL DplcapMOD D (CJO=3.8e-10 IS=1.0e-30 N=10 M=0.60)

.MODEL MmedMOD NMOS (VTO=3.6 KP=3 IS=1e-40 N=10 TOX=1 L=1u W=1u RG=1.5)

.MODEL MstroMOD NMOS (VTO=4.3 KP=59 IS=1e-30 N=10 TOX=1 L=1u W=1u)

.MODEL MweakMOD NMOS (VTO=3.09 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=15 RS=0.1)

.MODEL RbreakMOD RES (TC1=9.0e-4 TC2=-1.0e-7)

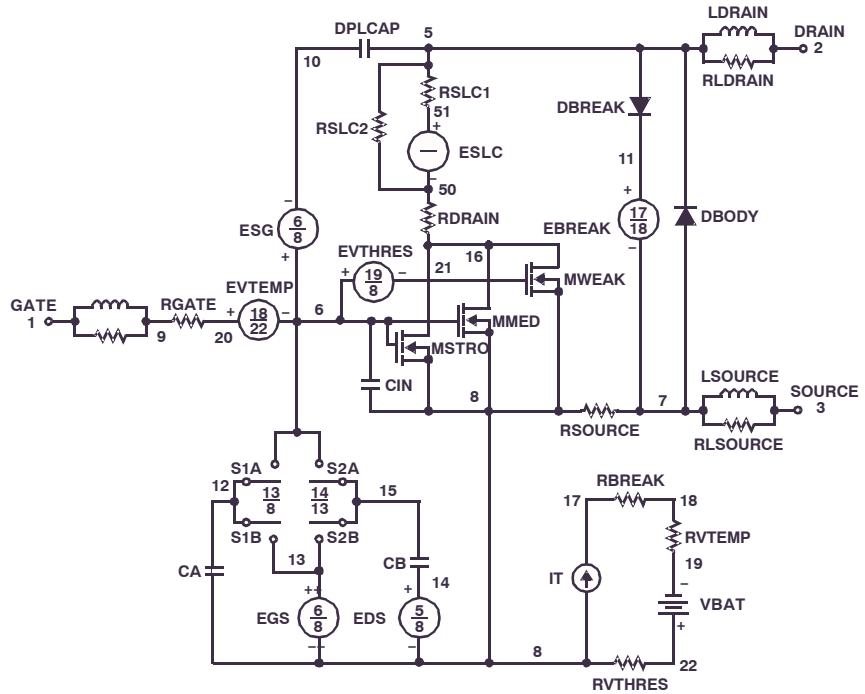
.MODEL RdrainMOD RES (TC1=11.0e-3 TC2= 6.1e-5)

.MODEL RSLCMOD RES (TC1=3.0e-3 TC2=1.0e-6)

.MODEL RsourceMOD RES (TC1=4.0e-3 TC2=1.0e-6)

.MODEL RvthresMOD RES (TC1=-3.5e-3 TC2=-1.5e-5)

.MODEL RvtempMOD RES (TC1=-4.3e-3 TC2=1.5e-6)



FDP3672

```
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.0 VOFF=-3.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-5.0)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.3)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.5)
```

.ENDS

For further discussion of the PSPICE model, consult *A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options*; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



Share Feedback
Your Opinion Matters

SPICE THERMAL MODEL

REV October 2002
FDP3672

CTHERM1 TH 6 3.2e-3
CTHERM2 6 5 3.3e-3
CTHERM3 5 4 3.4e-3
CTHERM4 4 3 3.5e-3
CTHERM5 3 2 6.4e-3
CTHERM6 2 TL 1.9e-2

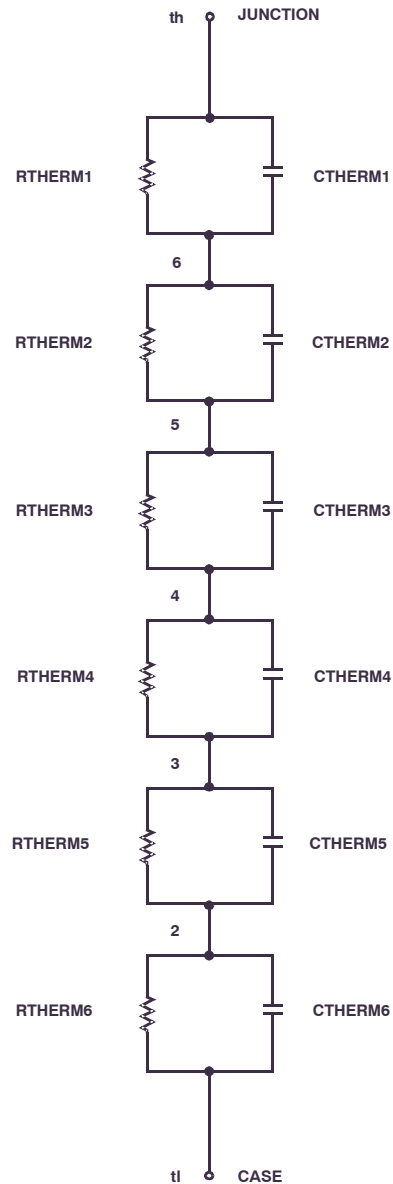
RTHERM1 TH 6 5.5e-4
RTHERM2 6 5 5.0e-3
RTHERM3 5 4 4.5e-2
RTHERM4 4 3 10.5e-2
RTHERM5 3 2 3.4e-1
RTHERM6 2 TL 3.5e-1

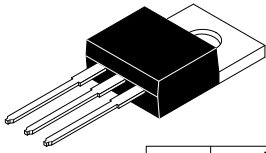
SABER THERMAL MODEL

SABER thermal model FDP3672
template thermal_model th tl
thermal_c th, tl

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  ctherm.ctherm2 6 5 =3.3e-3
  ctherm.ctherm3 5 4 =3.4e-3
  ctherm.ctherm4 4 3 =3.5e-3
  ctherm.ctherm5 3 2 =6.4e-3
  ctherm.ctherm6 2 tl =1.9e-2
```

```
  rtherm.rtherm1 th 6 =5.5e-4
  rtherm.rtherm2 6 5 =5.0e-3
  rtherm.rtherm3 5 4 =4.5e-2
  rtherm.rtherm4 4 3 =10.5e-2
  rtherm.rtherm5 3 2 =3.4e-1
  rtherm.rtherm6 2 tl =3.5e-1
}
```





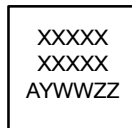
TO-220-3LD
CASE 340AT
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
θ	3°	--	5°

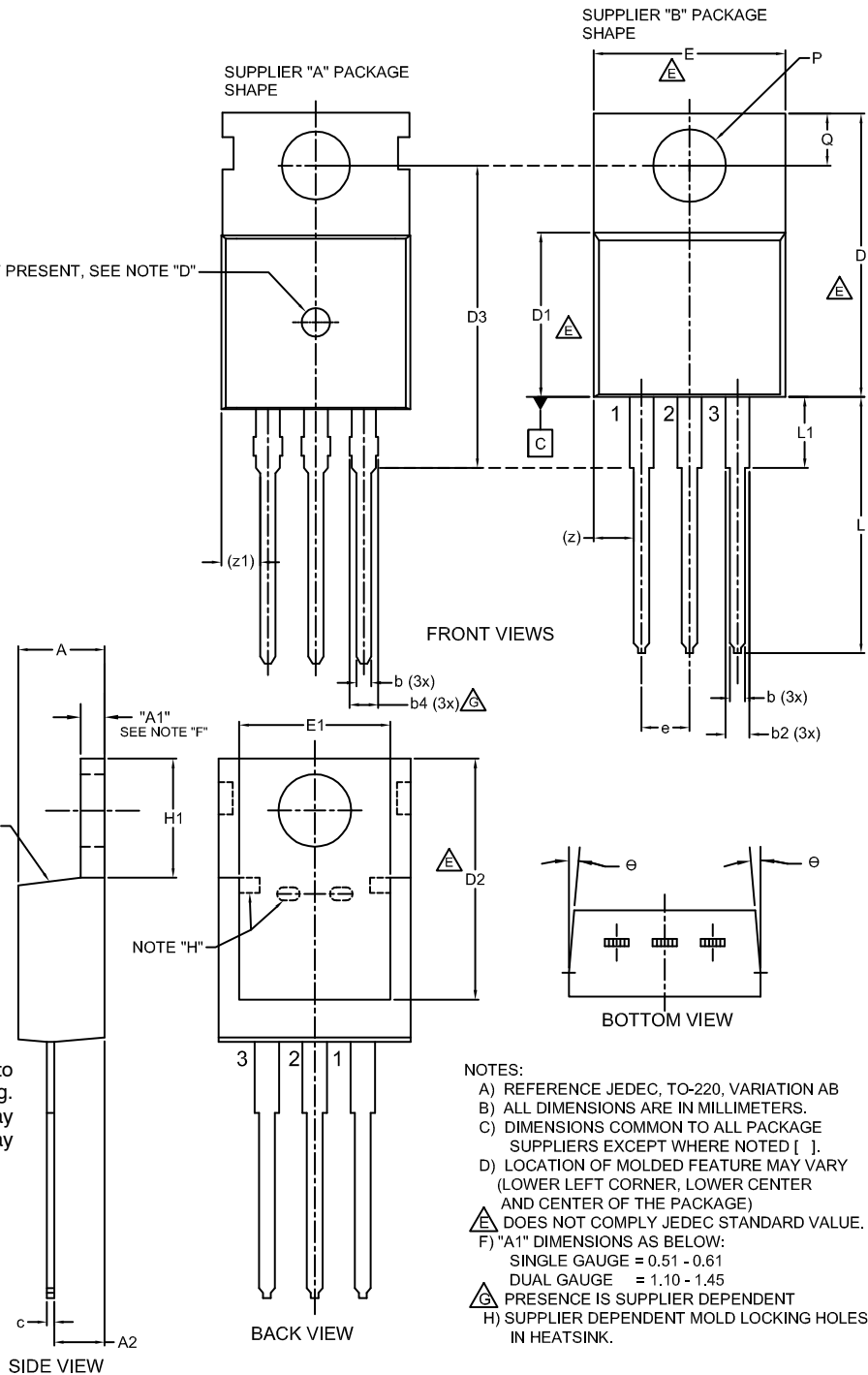
IF PRESENT, SEE NOTE "D"

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



NOTES:

- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- △ DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
- △ PRESENCE IS SUPPLIER DEPENDENT
- H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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