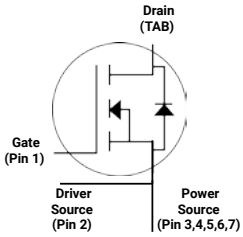
# C3M0280090J

## Silicon Carbide Power MOSFET C3M™ MOSFET Technology
## N-Channel Enhancement Mode


### Features

- New C3M Silicon Carbide (SiC) MOSFET technology
- High blocking voltage with low On-resistance
- High speed switching with low capacitances
- New low impedance package with driver source
- Fast intrinsic diode with low reverse recovery ($Q_{rr}$)
- Halogen free, RoHS compliant
- Wide creepage (~7mm) between drain and source

| Part Number | Package |
|---|---|
| C3M0280090J | TO-263-7 |

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### Typical Applications

- Renewable energy
- Lighting
- High voltage DC/DC converters
- Telecom Power Supplies
- Induction Heating

### Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency

### Key Parameters

| Parameter | Symbol | Min. | Typ. | Max | Unit | Conditions | Note |
|---|---|---|---|---|---|---|---|
| Drain - Source Voltage | $V_{DS}$ | | | 900 | v | $T_C$ = 25°C | |
| Maximum Gate - Source Voltage | $V_{GS(max)}$ | -8 | | +19 | | Transient | |
| Operational Gate-Source Voltage | $V_{GS\ op}$ | | -4/15 | | | Static | Note 1 |
| DC Continuous Drain Current | $I_D$ | | | 11 | A | $V_{GS}$ = 15 V, $T_C$ = 25 °C, $T_J$ ≤150 °C | Fig. 19 Note 2 |
| | | | | 7 | | $V_{GS}$ = 15 V, $T_C$ = 100 °C, $T_J$ ≤150 °C | |
| Pulsed Drain Current | $I_{DM}$ | | | 22 | | $t_{Pmax}$ limited by $T_{jmax}$ $V_{GS}$ = 15V, $T_C$ = 25 °C | Fig. 22 |
| Power Dissipation | $P_D$ | | | 49 | W | $T_C$ = 25 °C, $T_J$ = 150 °C | Fig. 20 |
| Operating Junction and Storage Temperature | $T_J$, $T_{stg}$ | | | -55 to +150 | °C | | |
| Solder Temperature | $T_L$ | | | 260 | | According to JEDEC J-STD-020 | |

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

## Electrical Characteristics ($T_C$ = 25℃ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | 900 | — | — | V | $V_{GS}$ = 0 V, $I_D$ = 100 µA | |
| Gate Threshold Voltage, $T_J$ = 25℃ | $V_{GS(th)}$ | 1.8 | 2.7 | 3.5 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.2 mA | Fig. 11 |
| Gate Threshold Voltage, $T_J$ = 150℃ | | — | 2.2 | — | | | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | — | 1 | 100 | µA | $V_{DS}$ = 900 V, $V_{GS}$ = 0 V | |
| Gate-Source Leakage Current | $I_{GSS}$ | — | 10 | 250 | nA | $V_{GS}$ = 15 V, $V_{DS}$ = 0 V | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | — | 320 | 360 | mΩ | $V_{GS}$ = 15 V, $I_D$ = 7.5 A, $T_J$ = 25°C | Fig. 4, 5, 6 |
| Drain-Source On-State Resistance | | — | 416 | — | | $V_{GS}$ = 15 V, $I_D$ = 7.5 A, $T_J$ = 150°C | |
| Transconductance | $g_{fs}$ | — | 3.6 | — | S | $V_{DS}$ = 20 V, $I_{DS}$ = 7.5 A, $T_J$ = 25°C | Fig. 7 |
| Transconductance | | | | | | $V_{GS}$ = 15 V, $I_D$ = 7.5 A, $T_J$ = 150°C | |
| Input Capacitance | $C_{iss}$ | — | 204 | — | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V<br>$f$ = 1 Mhz<br>$V_{AC}$ = 25 mV | Fig. 17, 18 |
| Output Capacitance | $C_{oss}$ | — | 26 | — | | | |
| Reverse Transfer Capacitance | $C_{rss}$ | — | 3 | — | | | |
| Output Capacitance Stored Energy | $E_{oss}$ | — | 5.5 | — | µJ | | Fig. 16 |
| Turn-On Switching Energy (Body Diode FWD) | $E_{on}$ | — | 18 | — | | $V_{DS}$ = 400 V, $V_{GS}$ = -4 V/15 V, $I_D$ = 7.5 A,<br>$R_{G(ext)}$ = 2.5 Ω, L= 201 µH, $T_J$ = 150°C | Fig. 26, 29 |
| Turn Off Switching Energy (Body Diode) | $E_{off}$ | — | 2.4 | — | | | |
| Turn-On Delay Time | $t_{d(on)}$ | — | 4 | — | ns | $V_{DD}$ = 400 V, $V_{GS}$ = -4 V/15 V<br>$I_D$ = 7.5 A, $R_{G(ext)}$ = 2.5 Ω,<br>Timing relative to $V_{DS}$<br>Inductive load | Fig. 27, 29 |
| Rise Time | $t_r$ | — | 7 | — | | | |
| Turn-Off Delay Time | $t_{d(off)}$ | — | | — | | | |
| Fall Time | $t_f$ | — | 4 | — | | | |
| Internal Gate Resistance | $R_{G(int)}$ | — | 23.5 | — | Ω | $f$ = 1 MHz, $V_{AC}$ = 25 mV | |
| Gate to Source Charge | $Q_{gs}$ | — | 4 | — | nC | $V_{DS}$ = 400 V, $V_{GS}$ = -4 V/15 V<br>$I_D$ = 7.5 A<br>Per IEC60747-8-4 pg 21 | Fig. 12 |
| Gate to Drain Charge | $Q_{gd}$ | — | 2 | — | | | |
| Total Gate Charge | $Q_g$ | — | 10 | — | | | |

## Reverse Diode Characteristics ($T_C$ = 25℃ unless otherwise specified)

| Parameter | Symbol | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| Diode Forward Voltage | $V_{SD}$ | 4.8 | — | V | $V_{GS}$ = -4 V, $I_{SD}$ = 4 A | Fig. 8, 9, 10 |
| | | 4.4 | — | | $V_{GS}$ = -4 V, $I_{SD}$ = 4 A, $T_J$ = 150°C | |
| Continuous Diode Forward Current | $I_S$ | — | 9 | A | $V_{GS}$ = -4 V | |
| Diode Pulse Current | $I_{S,\ pulsed}$ | — | 22 | | $V_{GS}$ = -4 V, pulse width $t_P$ limited by $T_{j\ max}$ | |
| Reverse Recover Time | $t_{rr}$ | 8 | — | nS | $V_{GS}$ = -4 V, $I_{SD}$ = 7.5 A, $V_R$ = 400 V<br>dif/dt = 2725 A/µs, $T_J$ = 150°C | |
| Reverse Recovery Charge | $Q_{rr}$ | 39 | — | nC | | |
| Peak Reverse Recovery Current | $I_{rrm}$ | 8 | — | A | | |

## Thermal Characteristics

| Parameter | Symbol | Max | Unit | Note |
|---|---|---|---|---|
| Thermal Resistance from Junction to Case | $R_{\theta JC}$ | 2.5 | °C/W | Fig. 21 |
| Thermal Resistance From Junction to Ambient | $R_{\theta JA}$ | 40 | | |

## Typical Performance

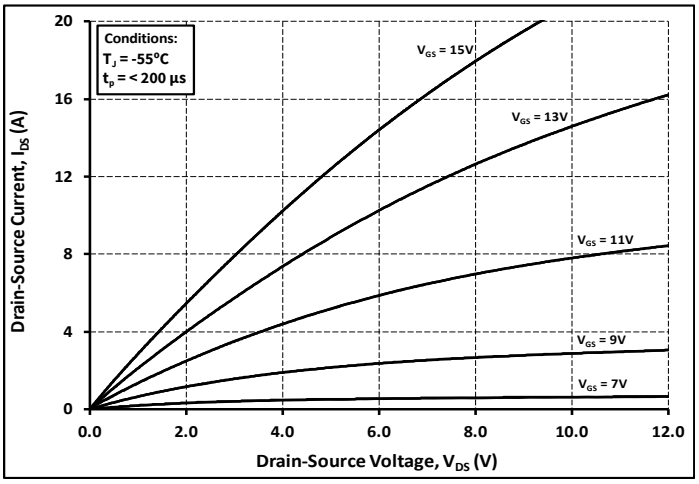



**Figure 1.** Output Characteristics $T_J$ = -55°C

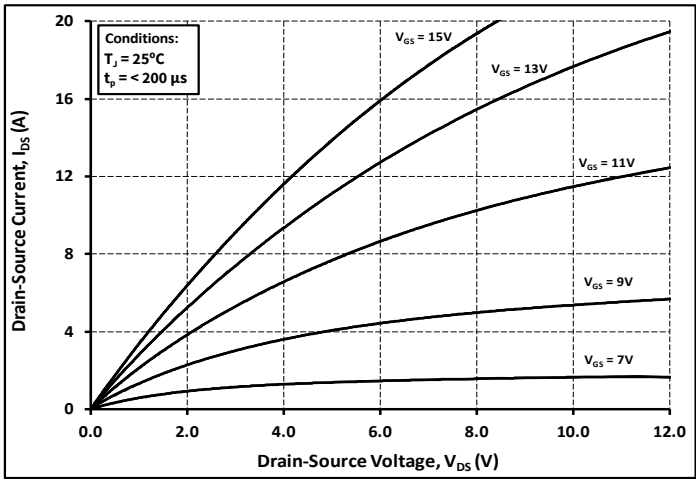



**Figure 2.** Output Characteristics $T_J$ = 25°C

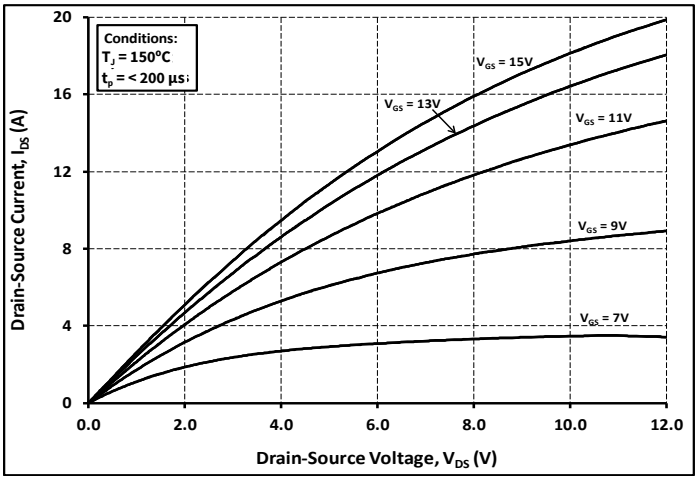



**Figure 3.** Output Characteristics $T_J$ = 150°C

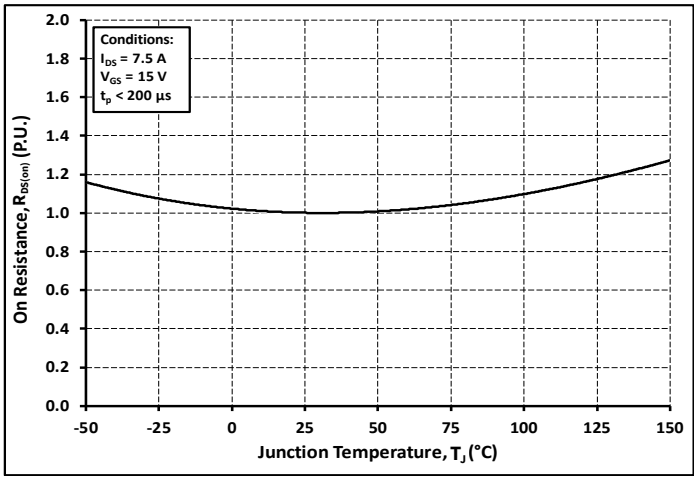



**Figure 4.** Normalized On-Resistance vs Temperature

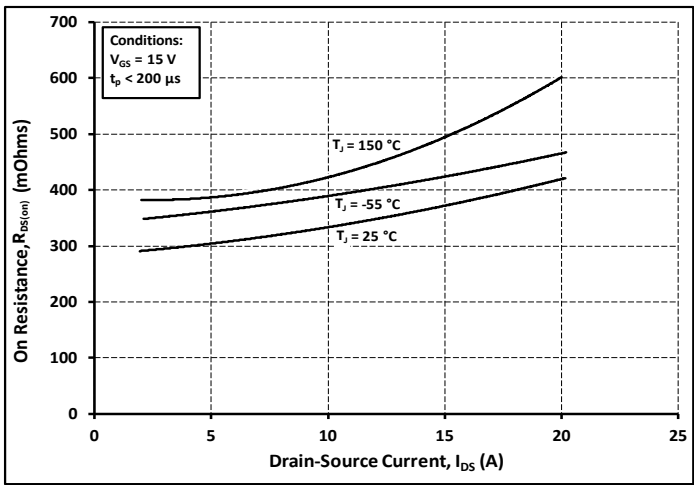



**Figure 5.** On-Resistance vs Drain Current For Various Temperatures

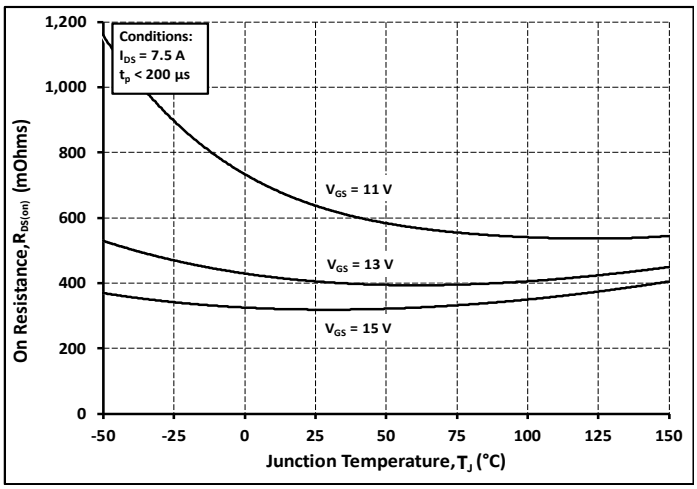



**Figure 6.** On-Resistance vs Temperature For Various Gate Voltage

## Typical Performance

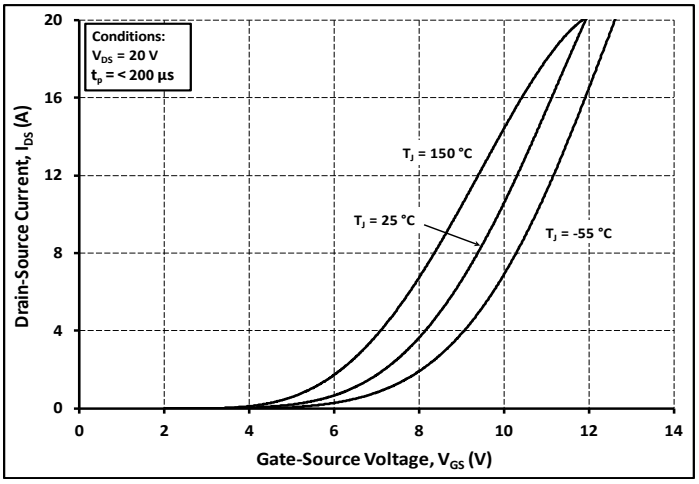



**Figure 7.** Transfer Characteristic for Various Junction Temperatures

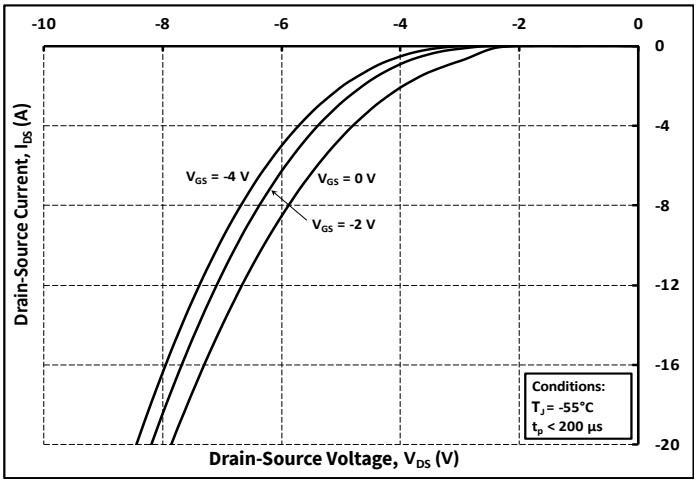



**Figure 8.** Body Diode Characteristic at -55°C

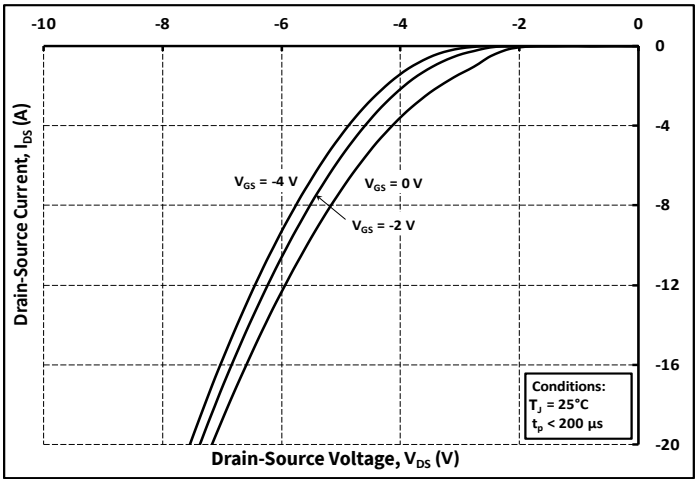



**Figure 9.** Body Diode Characteristic at 25°C

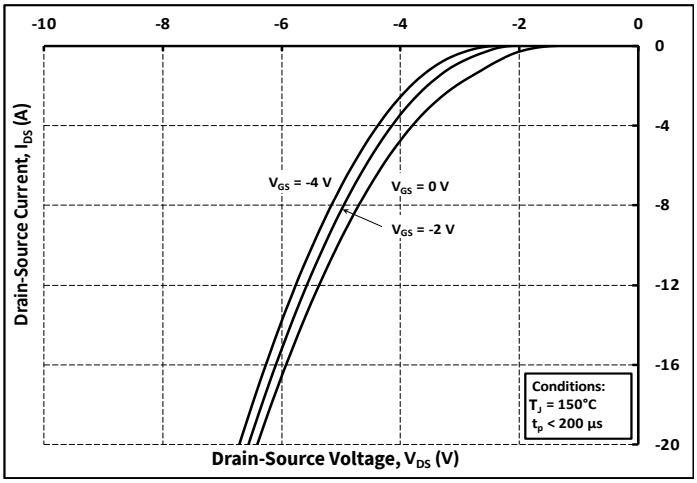



**Figure 10.** Body Diode Characteristic at 150°C

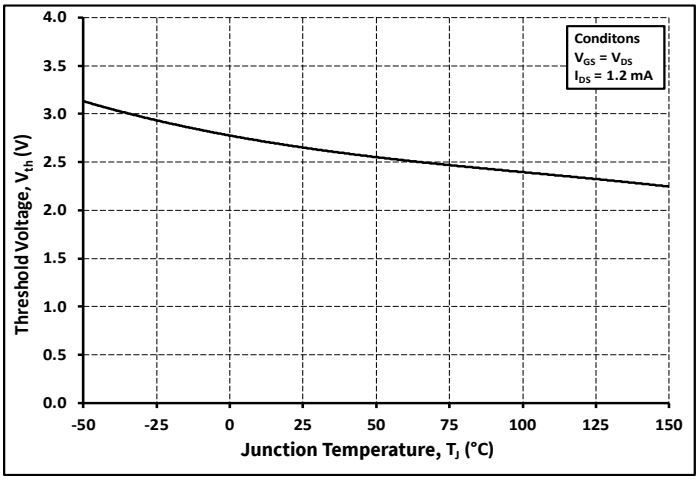



**Figure 11.** Threshold Voltage vs Temperature

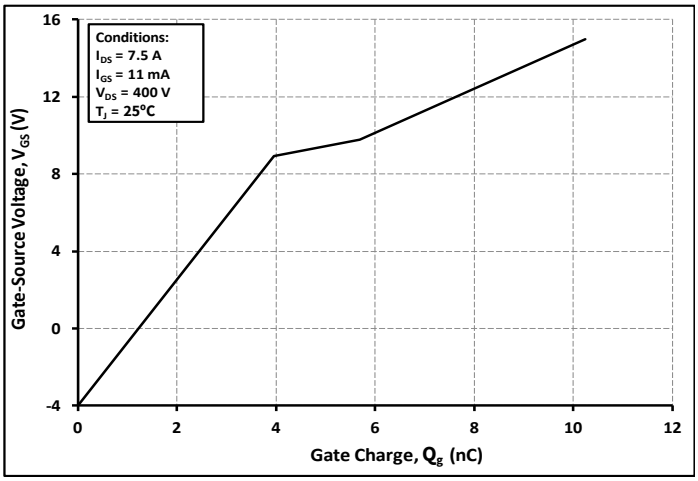



**Figure 12.** Gate Charge Characteristics

## Typical Performance

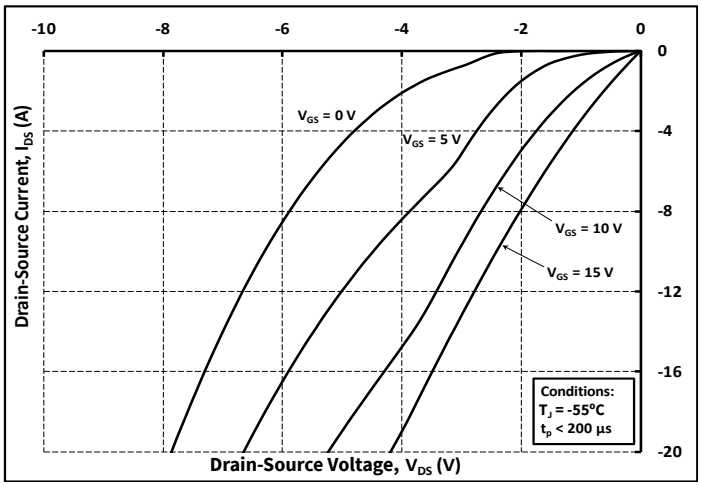



**Figure 13.** 3rd Quadrant Characteristic at -55°C

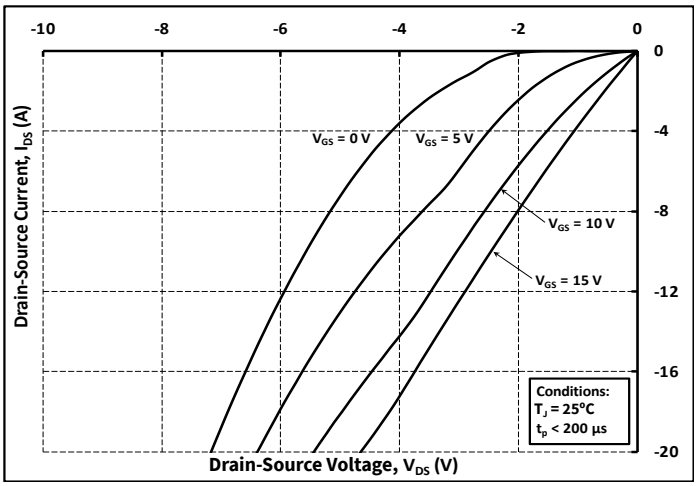



**Figure 14.** 3rd Quadrant Characteristic at 25°C

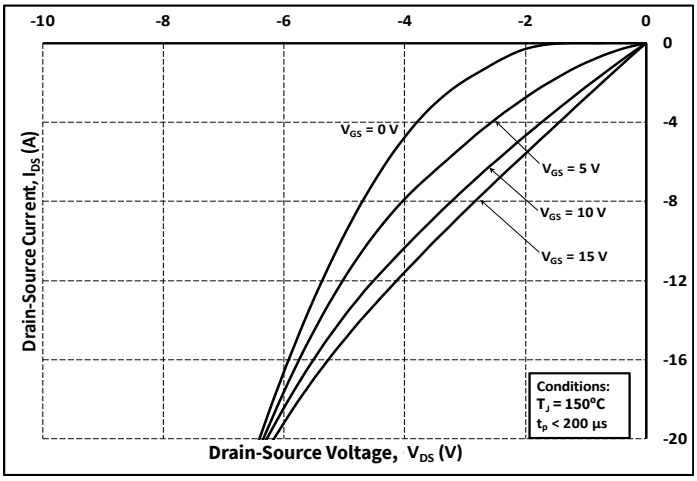



**Figure 15.** 3rd Quadrant Characteristic at 150°C

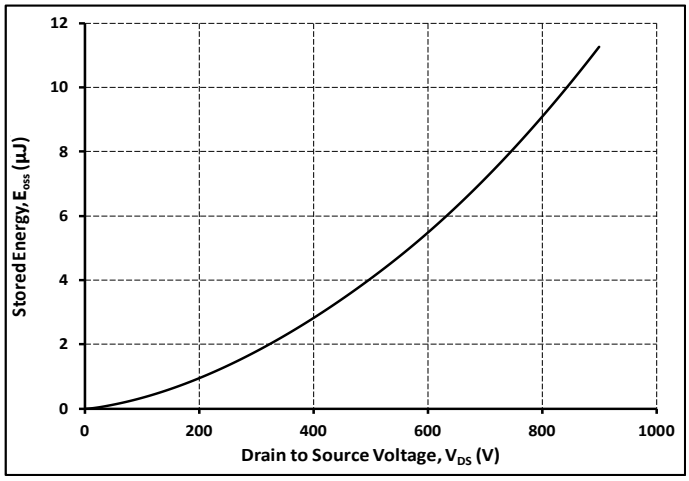



**Figure 16.** Output Capacitor Stored Energy

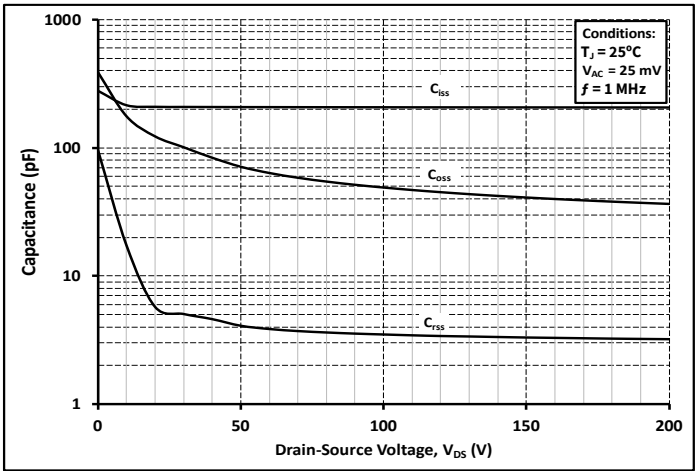



**Figure 17.** Capacitances vs Drain-Source Voltage (0 - 200 V)

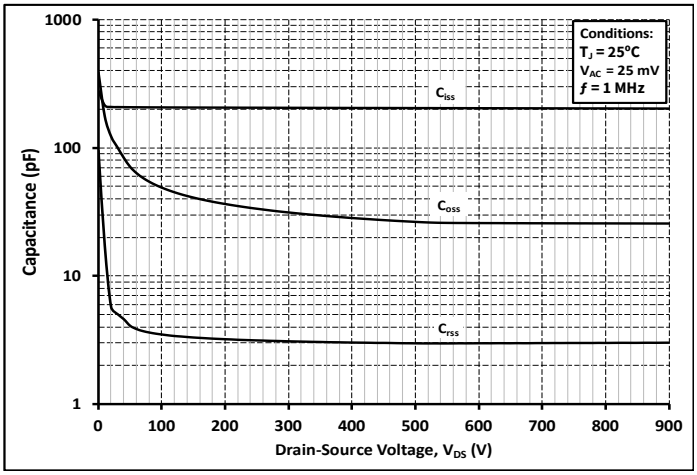



**Figure 18.** Capacitances vs Drain-Source Voltage (0 - 900 V)

## Typical Performance

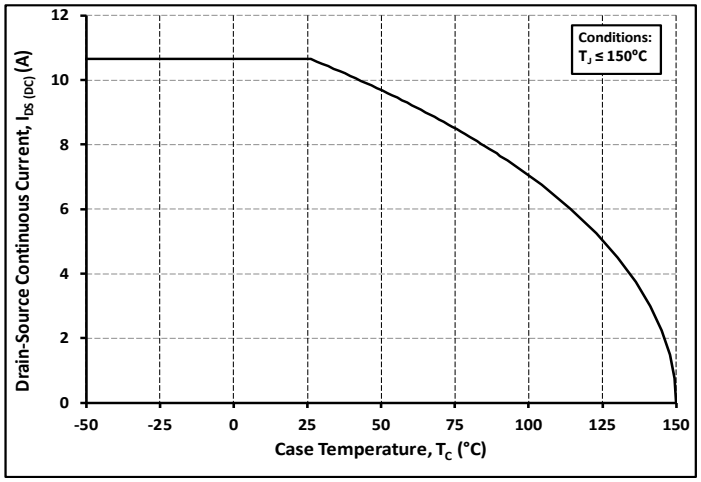



**Figure 19.** Continuous Drain Current Derating vs Case Temperature

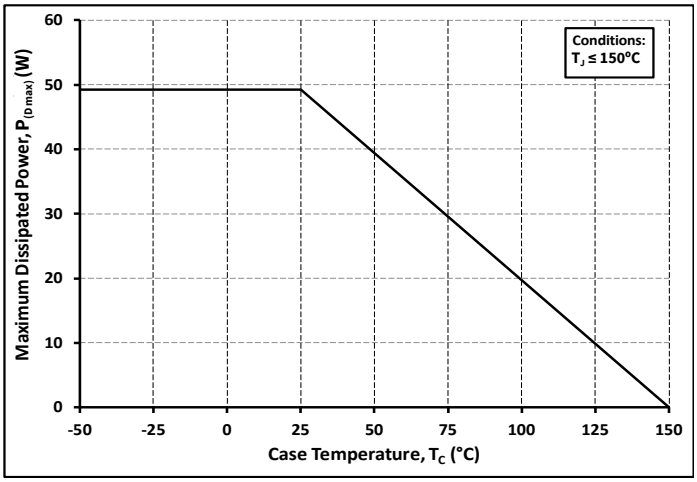



**Figure 20.** Maximum Power Dissipation Derating vs Case Temperature

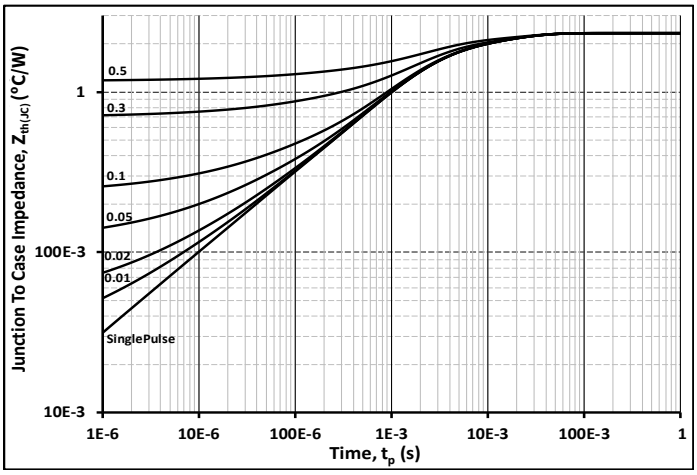



**Figure 21.** Transient Thermal Impedance (Junction - Case)

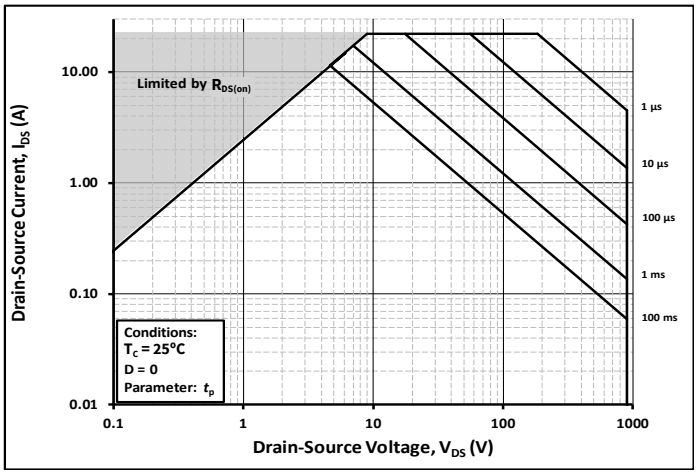



**Figure 22.** Safe Operating Area

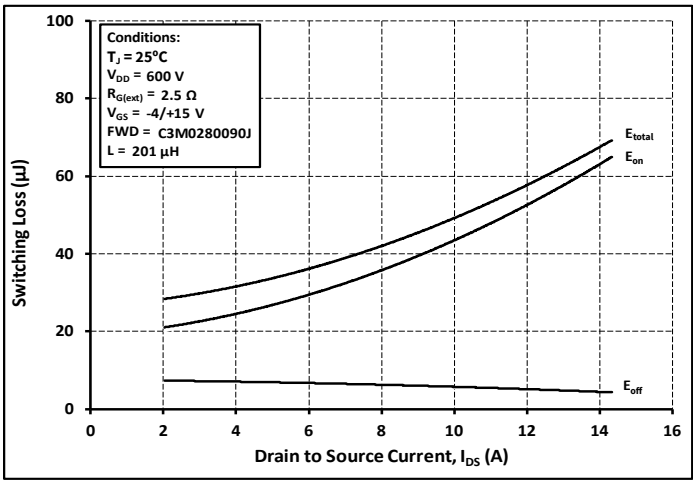



**Figure 23.** Clamped Inductive Switching Energy vs Drain Current ($V_{DD}$ = 600 V)

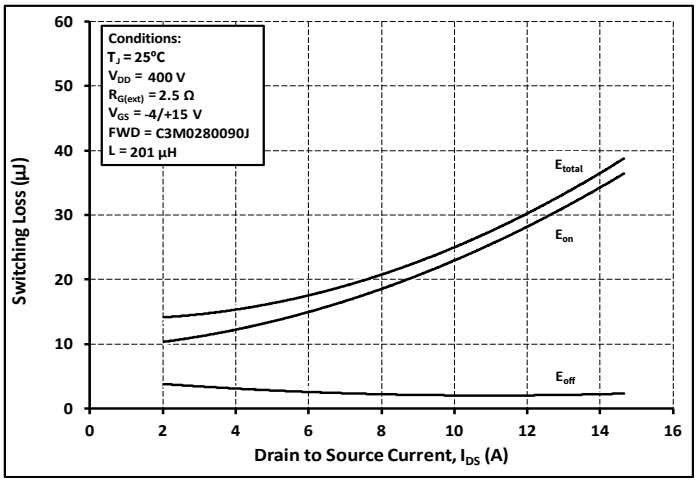



**Figure 24.** Clamped Inductive Switching Energy vs Drain Current ($V_{DD}$ = 400 V)

## Typical Performance

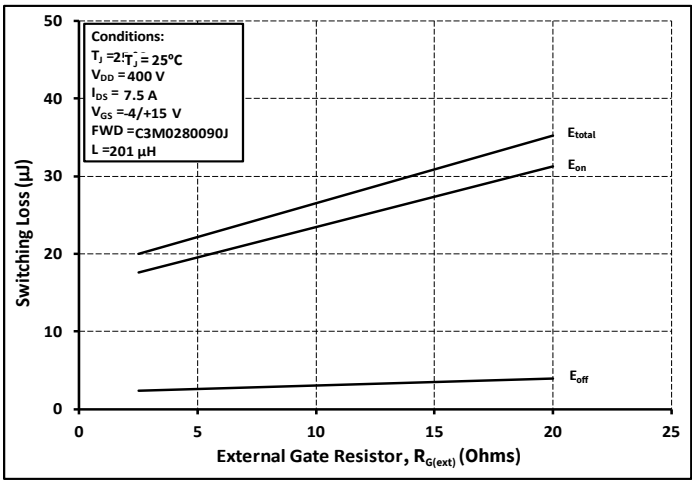



**Figure 25.** Clamped Inductive Switching Energy vs $R_{G(ext)}$

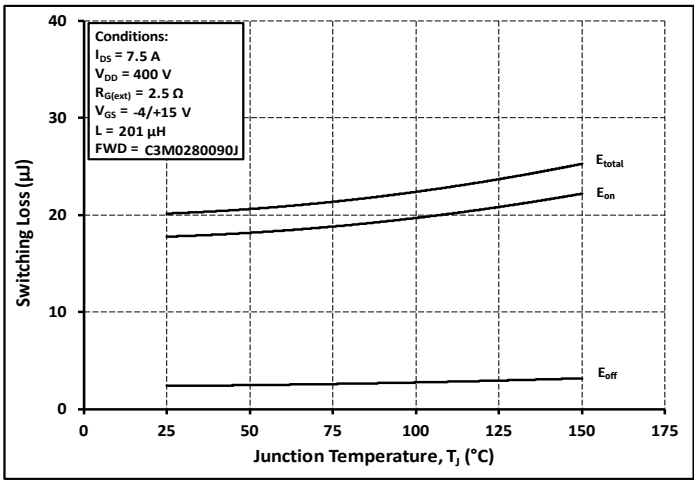



**Figure 26.** Clamped Inductive Switching Energy vs Temperature

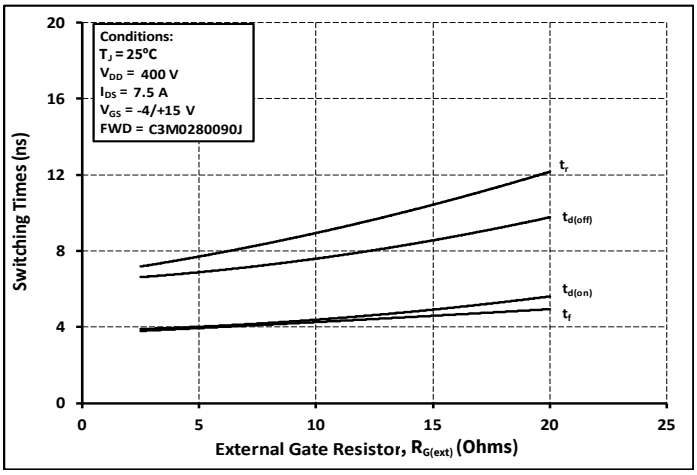



**Figure 27.** Switching Times vs. $R_{G(ext)}$

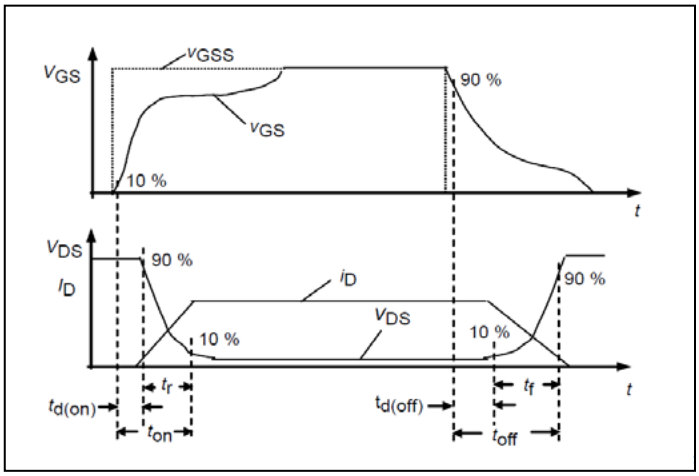



**Figure 28.** Switching Times Definition

## Test Circuit Schematic

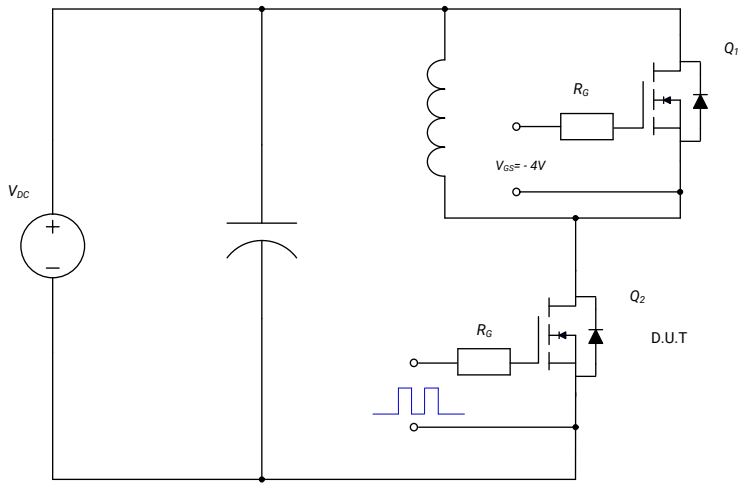
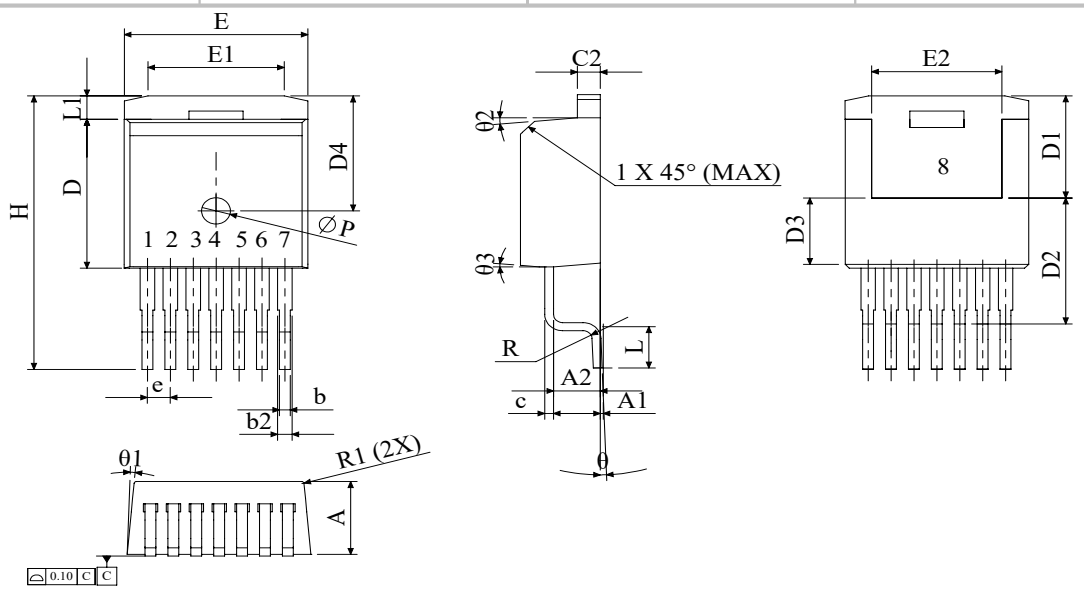



**Figure 29.** Clamped Inductive Switching Test Circuit

Note:
Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

## Package Dimensions – Package 7L D2PAK




| SYMBOL | MIN (mm) | MAX (mm) |
|---|---|---|
| A | 4.30 | 4.57 |
| A1 | 0.00 | 0.25 |
| b | 0.50 | 0.70 |
| b2 | 0.60 | 1.00 |
| c | 0.33 | 0.65 |
| C2 | 1.17 | 1.40 |
| D | 9.025 | 9.125 |
| D1 | 4.70 | 4.90 |
| D2 | 7.170 REF | |
| D3 | 4.000 REF | |
| D4 | 7.000 REF | |
| A2 | 2.595 REF | |
| E | 10.13 | 10.23 |
| E1 | 6.50 | 8.60 |
| E2 | 6.778 | 7.665 |
| e | 1.27 TYP | |
| H | 15.043 | 17.313 |
| L | 2.324 | 2.700 |
| L1 | 0.968 | 1.868 |
| R | 0.506 REF | |
| R1 | 0.500 REF | |
| θ | 0° | 8° |
| θ1 | 4.5° | 5.5° |
| θ2 | 4° | 6° |
| θ3 | 4° | 6° |

| | |
|---|---|
| 1 | GATE |
| 2 | KELVIN |
| 3 | SOURCE |
| 4 | |
| 5 | |
| 6 | |
| 7 | |
| 8 | DRAIN |

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

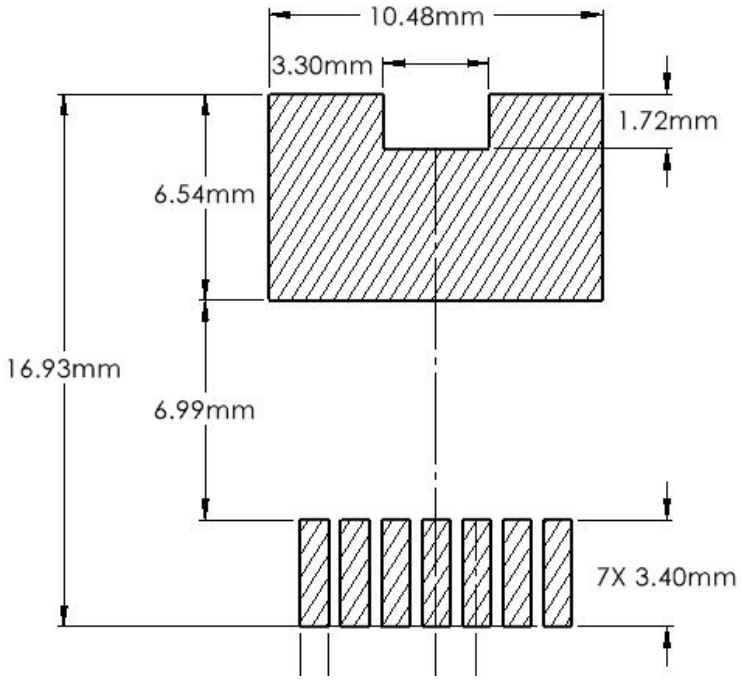
Wolfspeed

TITLE: PACKAGE OUTLINE DRAWING: TO 263-7L J

REVISION NO. 01 | A4

Date: 04/13/22 | SCALE:1:1 | SHEET 1 OF 1

## Recommended Solder Pad Layout




## Revision History

| Current Revision | Date of Release | Description of Changes |
|---|---|---|
| 2 | September-2021 | N/A |
| 3 | January-2024 | Updated Wolfspeed branding, package drawing, package image, solder pad layout, added Rev history, Table 1 layout revised |
| 4 | December - 2024 | Legal Disclaimer Updated |

## Related Links

- SiC MOSFET Isolated Gate Driver reference design
- SiC MOSFET Evaluation Board

## Notes & Disclaimer

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**Contact info:**

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power